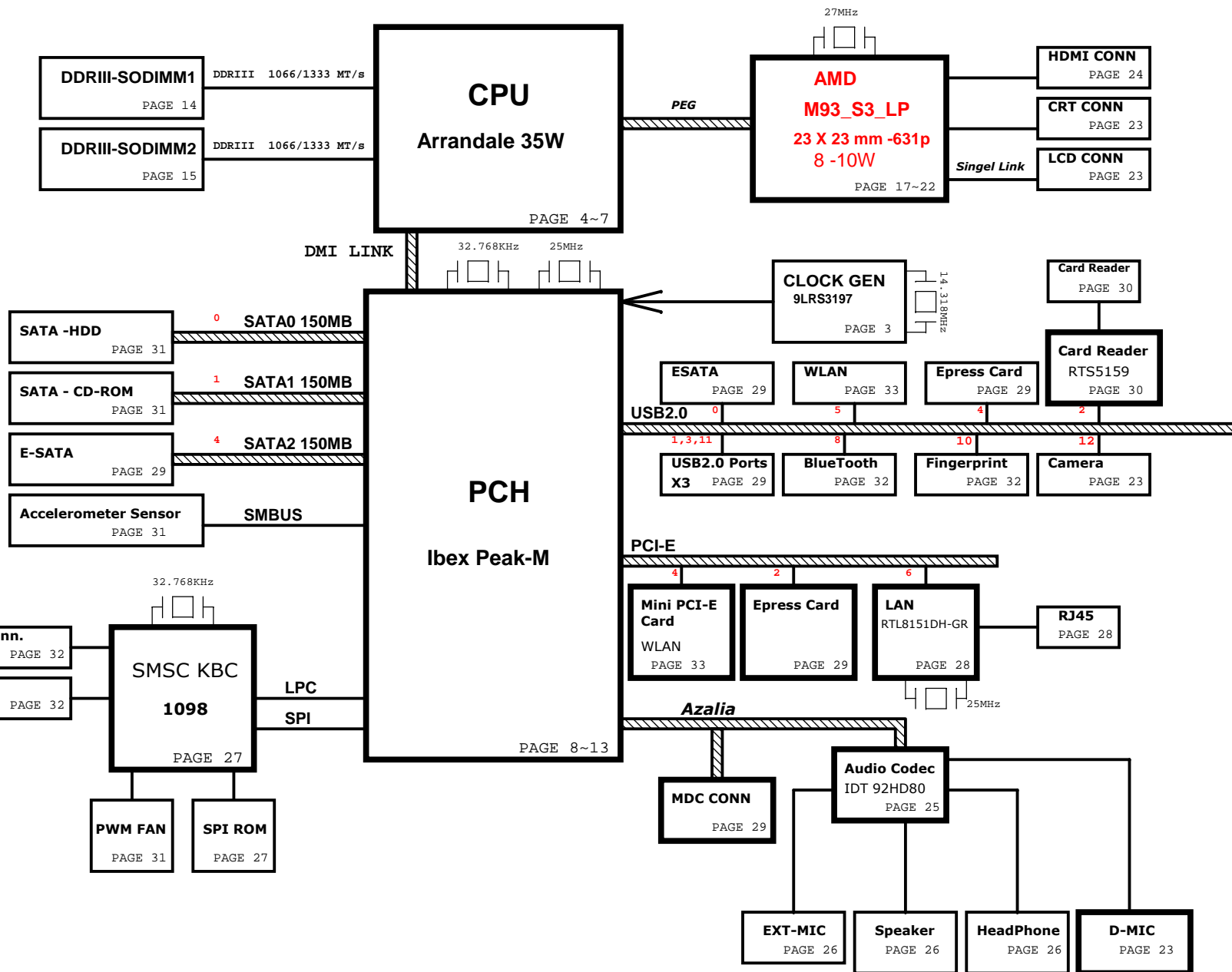


# Hamilton 1.0 ( SX6-DIS ) BLOCK DIAGRAM

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : IN3  
LAYER 7 : SGND  
LAYER 8 : BOT



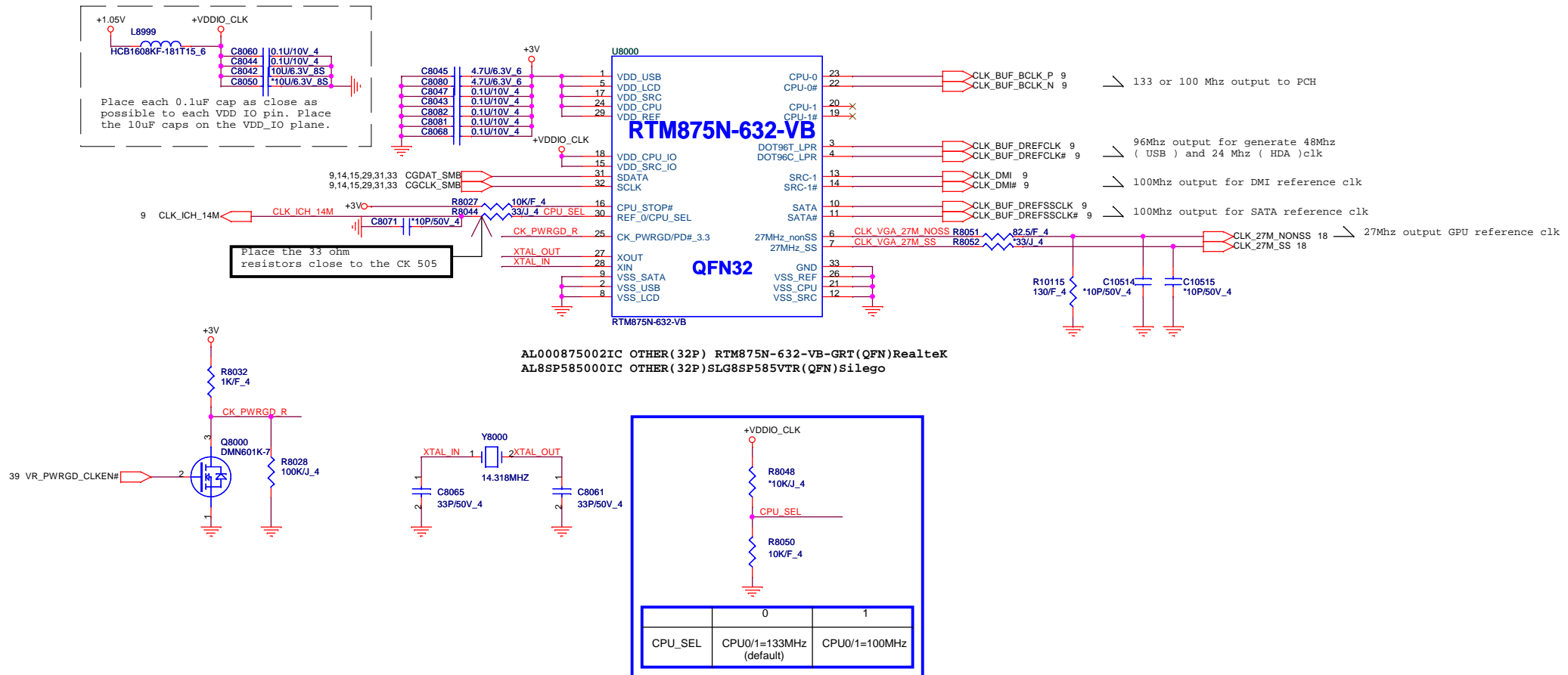
power State	+RTC_CELL	+VIN +3VPCU	+3VS5 +5VS5	+5VSUS +1.5VSUS	+5V +3V +1.8V_GFX +1.8V +1.5V +1.5V_CPU +1.1V_VTT +1.05V +1.0V_GFX +VGA_CORE +VCORE
S0	ON	ON	ON	ON	ON
S1	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4/S5 AC	ON	ON	ON	OFF	OFF
S4/S5 DC Only	ON	ON	OFF	OFF	OFF
AC/DC No Exist	ON	OFF	OFF	OFF	OFF

	SOURCE	BATTERY 0x16	CLK GEN 0xD2	Thermal IC 0x98(Write) / 0x99(Read)	G-SENSOR 0x3A(Write) /0x3B(Read)	WLAN	SO-DIMM DIMM0: 0xA0 DIMM1: 0xA2	SMSC 1098	GPU thermal sensor
SMBCLK SMBDATA	PCH	X	Y	Y	Y	Y	Y	X	X
SMB_CLK_ME1 SMB_DAT_ME1	PCH	X	X	X	X	X	X	Y	Y
AB1A_CLK AB1A_DATA	SMSC 1098	Y	X	X	X	X	X	X	X



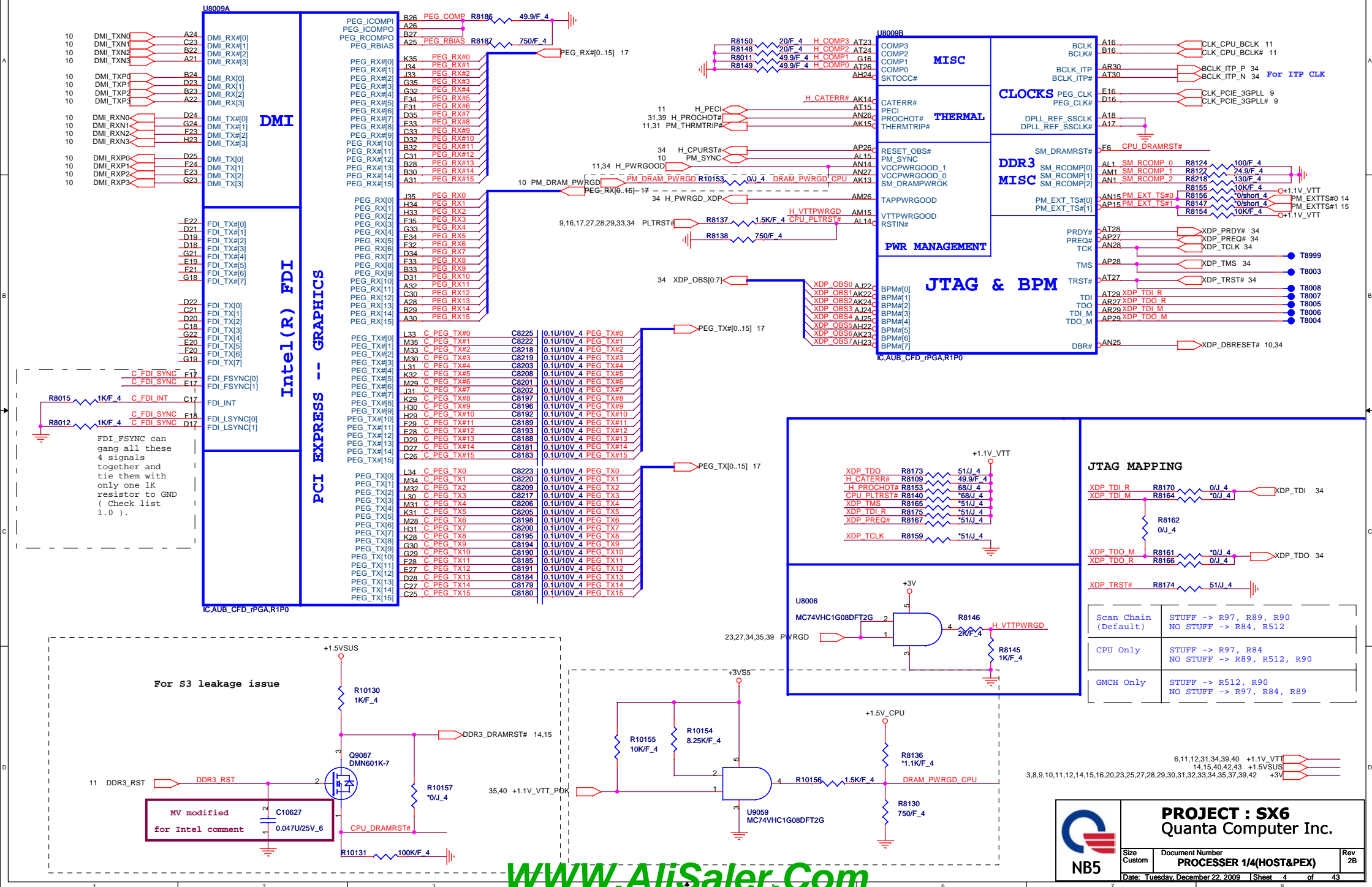
**PROJECT : SX6**  
Quanta Computer Inc.

Size Custom	Document Number <b>power rails</b>	Rev 2B
Date: Tuesday, December 15, 2009   Sheet 2 of 43		



**PROJECT : SX6**  
 Quantas Computer Inc.

Size Custom	Document Number <b>CLOCK GEN (9LRS3197)</b>	Rev 2B
Date: Tuesday, December 15, 2009	Sheet 3 of 43	



The diagram illustrates the pinout for two chips, U8009C and U8009D, which are DDR SYSTEM MEMORY A and B respectively. The chips are shown in a side-by-side layout, with their respective pin numbers and functions listed on the left and right sides.

**U8009C (DDR SYSTEM MEMORY A) Pinout:**

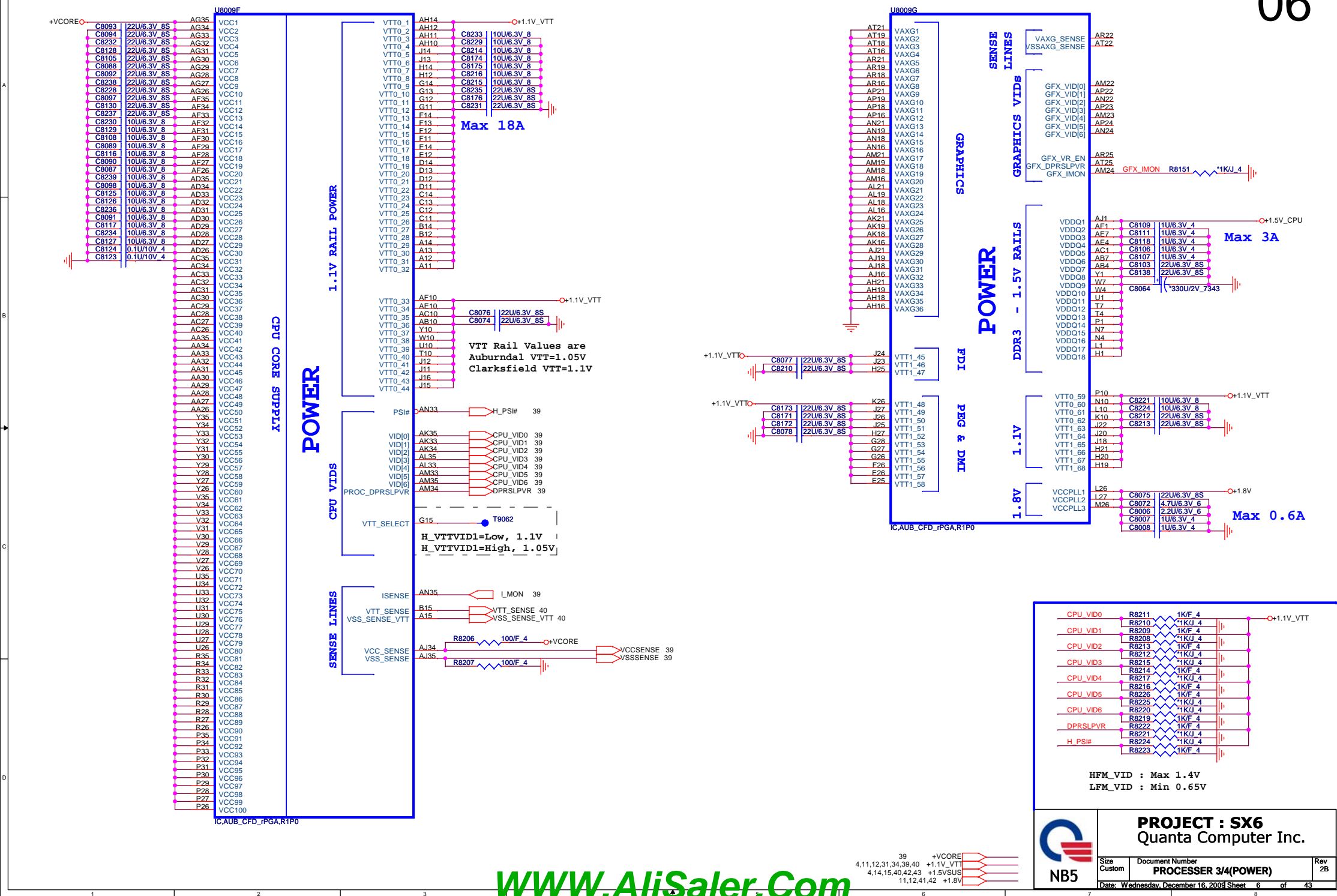
- Pin 1:** M\_A DQ0 A10
- Pin 2:** M\_A DQ1 C10
- Pin 3:** M\_A DQ2 C7
- Pin 4:** M\_A DQ3 A7
- Pin 5:** M\_A DQ4 B10
- Pin 6:** M\_A DQ5 E10
- Pin 7:** M\_A DQ7 A8
- Pin 8:** M\_A DQ8 D8
- Pin 9:** M\_A DQ9 F10
- Pin 10:** M\_A DQ10 E6
- Pin 11:** M\_A DQ11 F7
- Pin 12:** M\_A DQ12 E9
- Pin 13:** M\_A DQ14 B7
- Pin 14:** M\_A DQ15 C6
- Pin 15:** M\_A DQ16 H10
- Pin 16:** M\_A DQ17 G8
- Pin 17:** M\_A DQ18 K7
- Pin 18:** M\_A DQ19 J6
- Pin 19:** M\_A DQ20 G7
- Pin 20:** M\_A DQ21 G10
- Pin 21:** M\_A DQ22 J7
- Pin 22:** M\_A DQ23 J10
- Pin 23:** M\_A DQ24 L7
- Pin 24:** M\_A DQ25 M6
- Pin 25:** M\_A DQ26 M8
- Pin 26:** M\_A DQ27 L9
- Pin 27:** M\_A DQ28 L6
- Pin 28:** M\_A DQ29 K8
- Pin 29:** M\_A DQ30 N8
- Pin 30:** M\_A DQ31 P9
- Pin 31:** M\_A DQ32 AF5
- Pin 32:** M\_A DQ33 AK6
- Pin 33:** M\_A DQ34 AK6
- Pin 34:** M\_A DQ35 AK7
- Pin 35:** M\_A DQ36 AF6
- Pin 36:** M\_A DQ37 AG5
- Pin 37:** M\_A DQ38 AJ7
- Pin 38:** M\_A DQ39 AJ6
- Pin 39:** M\_A DQ40 AJ10
- Pin 40:** M\_A DQ41 AJ9
- Pin 41:** M\_A DQ42 AL10
- Pin 42:** M\_A DQ43 AK12
- Pin 43:** M\_A DQ44 AK8
- Pin 44:** M\_A DQ45 AL7
- Pin 45:** M\_A DQ46 AL8
- Pin 46:** M\_A DQ48 AN8
- Pin 47:** M\_A DQ49 AM10
- Pin 48:** M\_A DQ50 AR11
- Pin 49:** M\_A DQ51 AL11
- Pin 50:** M\_A DQ52 AN9
- Pin 51:** M\_A DQ53 AT11
- Pin 52:** M\_A DQ55 AP12
- Pin 53:** M\_A DQ56 AM12
- Pin 54:** M\_A DQ57 AN12
- Pin 55:** M\_A DQ58 AM13
- Pin 56:** M\_A DQ59 AT14
- Pin 57:** M\_A DQ60 AL13
- Pin 58:** M\_A DQ62 AR14
- Pin 59:** M\_A DQ63 AP14
- Pin 60:** M\_A DQ63 AP14

**U8009D (DDR SYSTEM MEMORY B) Pinout:**

- Pin 1:** M\_B DQ0 B5
- Pin 2:** M\_B DQ1 A5
- Pin 3:** M\_B DQ2 C3
- Pin 4:** M\_B DQ3 B3
- Pin 5:** M\_B DQ4 E4
- Pin 6:** M\_B DQ5 A4
- Pin 7:** M\_B DQ7 C4
- Pin 8:** M\_B DQ8 D1
- Pin 9:** M\_B DQ9 D2
- Pin 10:** M\_B DQ10 F2
- Pin 11:** M\_B DQ11 F1
- Pin 12:** M\_B DQ12 C2
- Pin 13:** M\_B DQ14 F5
- Pin 14:** M\_B DQ15 F4
- Pin 15:** M\_B DQ16 H4
- Pin 16:** M\_B DQ17 G2
- Pin 17:** M\_B DQ18 J2
- Pin 18:** M\_B DQ19 J6
- Pin 19:** M\_B DQ20 G5
- Pin 20:** M\_B DQ21 G1
- Pin 21:** M\_B DQ22 J2
- Pin 22:** M\_B DQ23 J1
- Pin 23:** M\_B DQ24 J5
- Pin 24:** M\_B DQ25 K2
- Pin 25:** M\_B DQ26 L3
- Pin 26:** M\_B DQ27 M1
- Pin 27:** M\_B DQ28 K5
- Pin 28:** M\_B DQ29 K4
- Pin 29:** M\_B DQ30 M4
- Pin 30:** M\_B DQ31 N5
- Pin 31:** M\_B DQ32 AF3
- Pin 32:** M\_B DQ33 AG1
- Pin 33:** M\_B DQ34 AJ3
- Pin 34:** M\_B DQ35 AK1
- Pin 35:** M\_B DQ36 AG4
- Pin 36:** M\_B DQ37 AG3
- Pin 37:** M\_B DQ38 AJ4
- Pin 38:** M\_B DQ39 AH4
- Pin 39:** M\_B DQ40 AK3
- Pin 40:** M\_B DQ41 AK4
- Pin 41:** M\_B DQ42 AM6
- Pin 42:** M\_B DQ43 AN2
- Pin 43:** M\_B DQ44 AK5
- Pin 44:** M\_B DQ46 AK2
- Pin 45:** M\_B DQ47 AM3
- Pin 46:** M\_B DQ48 AP3
- Pin 47:** M\_B DQ49 AN5
- Pin 48:** M\_B DQ50 AT4
- Pin 49:** M\_B DQ51 AN6
- Pin 50:** M\_B DQ52 AN5
- Pin 51:** M\_B DQ53 AN3
- Pin 52:** M\_B DQ54 AT5
- Pin 53:** M\_B DQ55 AN7
- Pin 54:** M\_B DQ56 AT6
- Pin 55:** M\_B DQ57 AP6
- Pin 56:** M\_B DQ58 AP8
- Pin 57:** M\_B DQ59 AT9
- Pin 58:** M\_B DQ60 AT7
- Pin 59:** M\_B DQ61 AP9
- Pin 60:** M\_B DQ62 AR10
- Pin 61:** M\_B DQ63 AT10

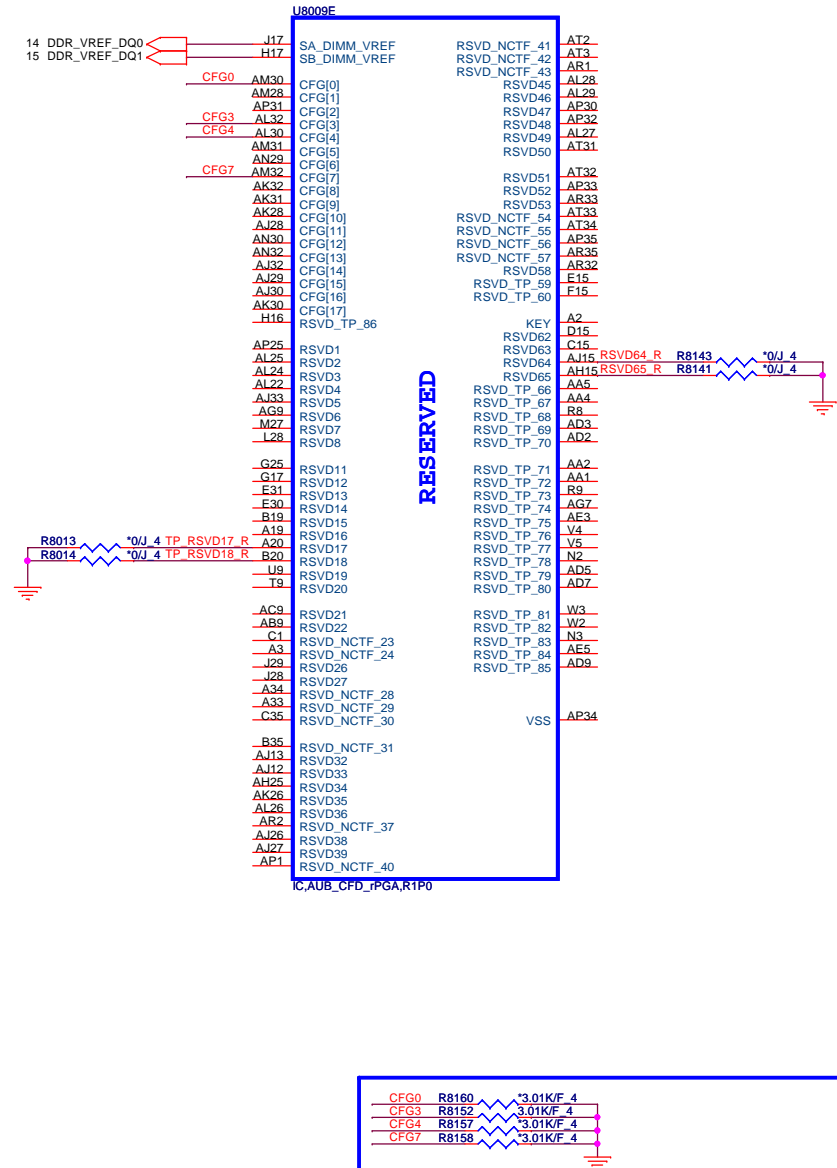
**Control Signals:**

- SA\_CLK[0]:** M\_A\_CLK0 14, M\_B\_CLK0 15
- SA\_CLK#:** M\_A\_CLK# 14, M\_B\_CLK# 15
- SA\_CKE[0]:** M\_A\_CKE0 14, M\_B\_CKE0 15
- SA\_CS[0]:** M\_A\_CS0 14, M\_B\_CS0 15
- SA\_CS#:** M\_A\_CS# 14, M\_B\_CS# 15
- SA\_ODT[0]:** M\_A\_ODT0 14, M\_B\_ODT0 15
- SA\_ODT#:** M\_A\_ODT# 14, M\_B\_ODT# 15
- SA\_DM[0]:** M\_A\_DM0 14, M\_B\_DM0 15
- SA\_DM#:** M\_A\_DM# 14, M\_B\_DM# 15
- SA\_DQS[0]:** M\_A\_DQS#0 14, M\_B\_DQS#0 15
- SA\_DQS#:** M\_A\_DQS# 14, M\_B\_DQS# 15
- SA\_DQ[0]:** M\_A\_DQ0 14, M\_B\_DQ0 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[1]:** M\_A\_DQ1 14, M\_B\_DQ1 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[2]:** M\_A\_DQ2 14, M\_B\_DQ2 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[3]:** M\_A\_DQ3 14, M\_B\_DQ3 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[4]:** M\_A\_DQ4 14, M\_B\_DQ4 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[5]:** M\_A\_DQ5 14, M\_B\_DQ5 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[6]:** M\_A\_DQ6 14, M\_B\_DQ6 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[7]:** M\_A\_DQ7 14, M\_B\_DQ7 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[8]:** M\_A\_DQ8 14, M\_B\_DQ8 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[9]:** M\_A\_DQ9 14, M\_B\_DQ9 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[10]:** M\_A\_DQ10 14, M\_B\_DQ10 15
- SA\_DQ#:** M\_A\_DQ# 14, M\_B\_DQ# 15
- SA\_DQ[11]:** M\_A\_DQ11 14, M\_B\_DQ11 15





**AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)**

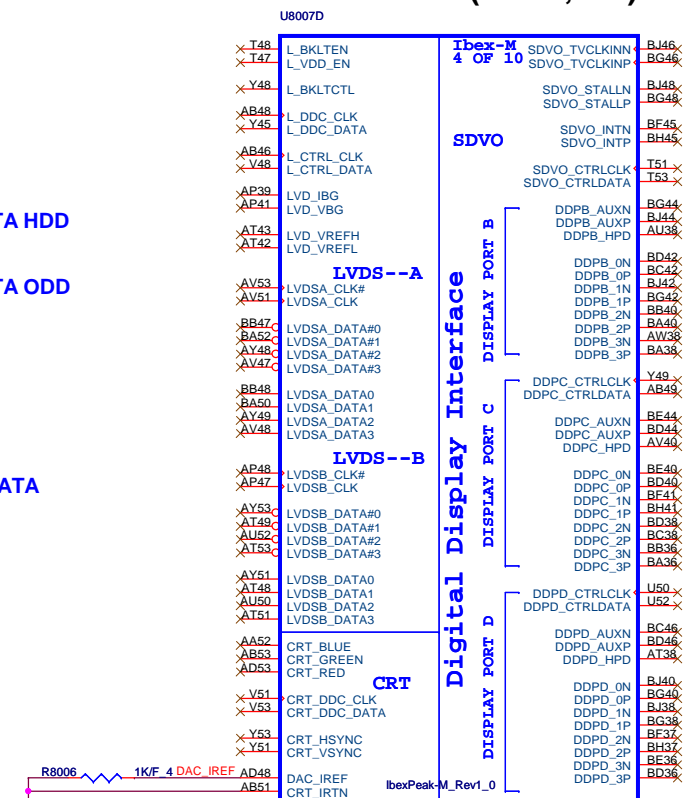


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Configuration Reveal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

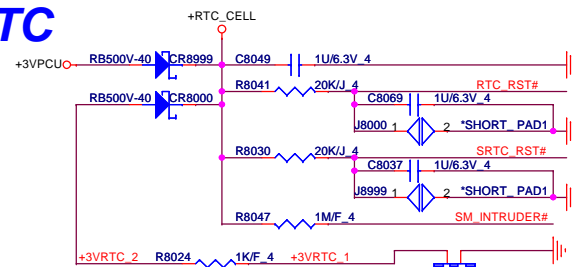


Size Custom	Document Number <b>PROCESSER 4/4(GND)</b>	Revised
Date: Tuesday, December 15, 2009		Sheet 7 of 43

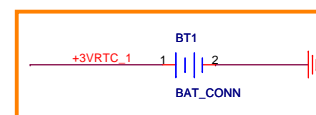
## IBEX PEAK-M (LVDS,DDI)



**RTC**



PV modified -

DFWF02MS022  
SI change p/r

8 9 10 11 12

3.9 10.12 34.39 41 +1.05

+1.05

1

1



Size

--	--

## Docum

ent Num

nber

---

---

---

---

Rev
-----

[illegible]

**For AUDIO**

**For MDC**



NB5

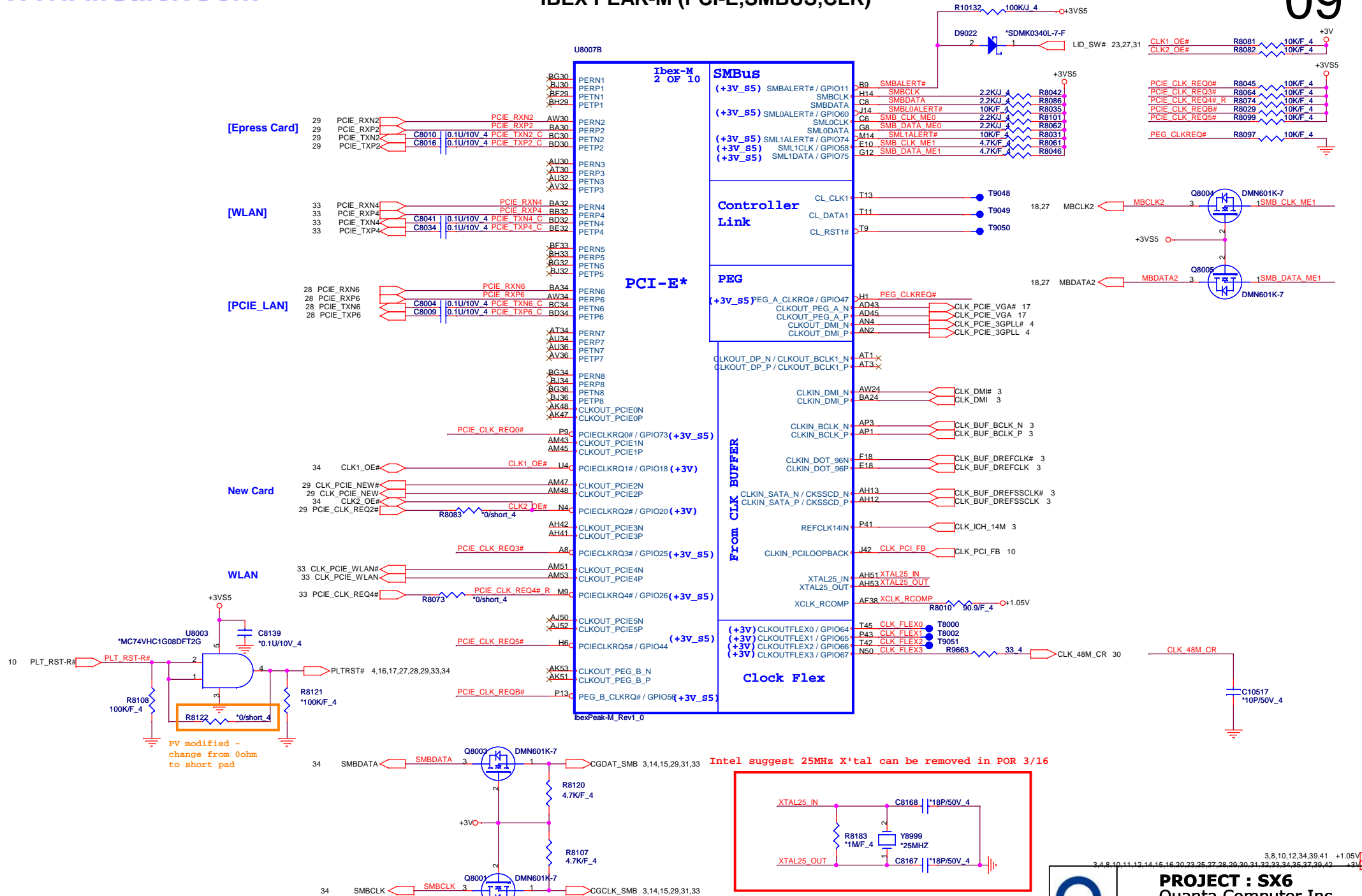
**PROJECT : SX6**  
Quanta Computer Inc.

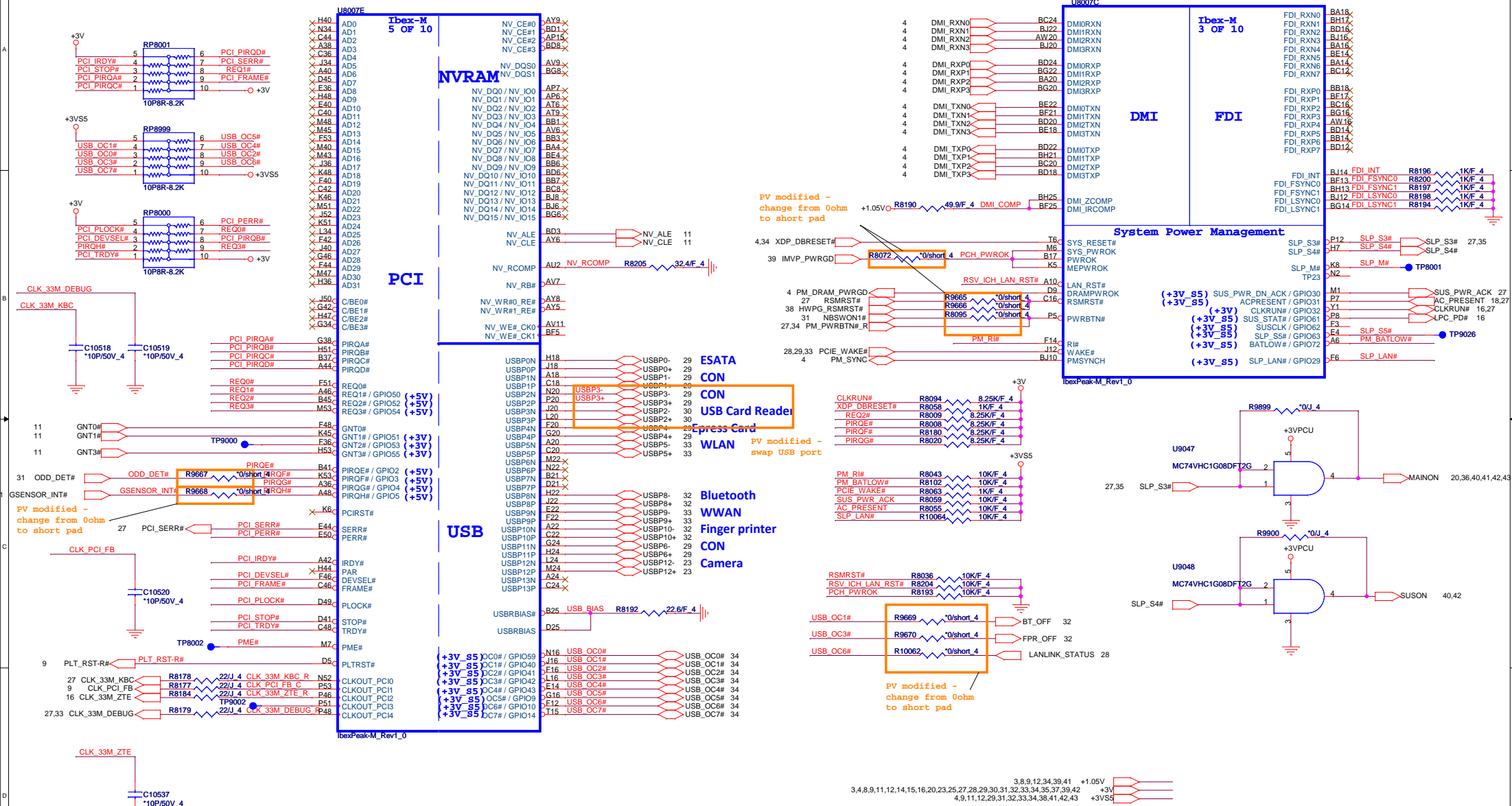
Size	Document Number	Rev
------	-----------------	-----

Custom	PCH 2/6 (SATA,HDA,LPC)	2B
--------	------------------------	----

Date: Tuesday, December 15, 2009      Sheet 8 of 43

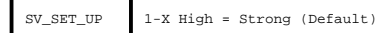
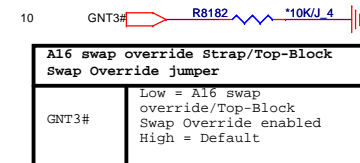
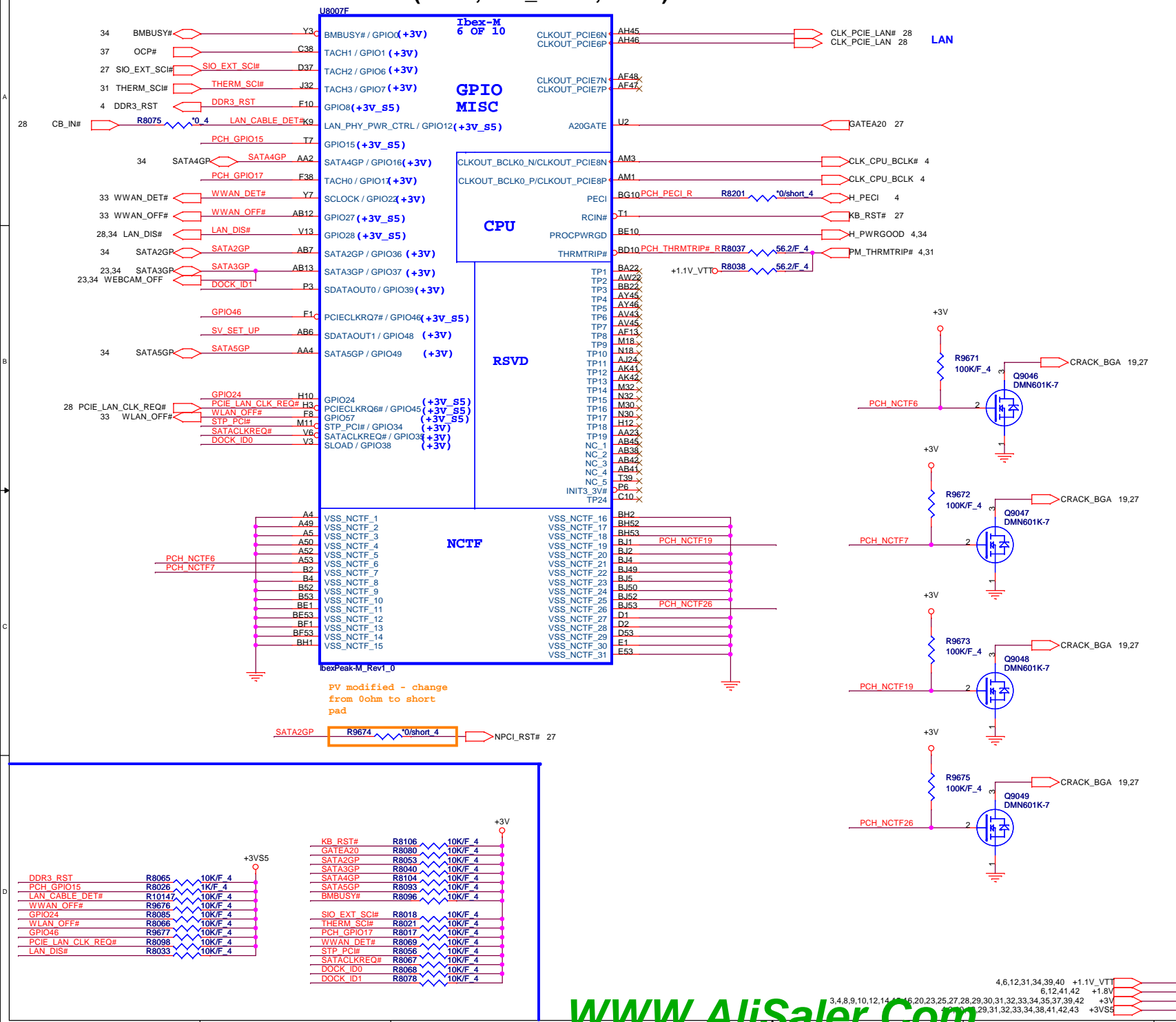






## IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

11



**Boot BIOS Strap**

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



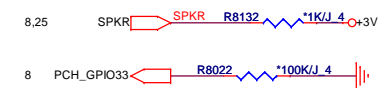
**Danbury Technology Enabled**

NV_ALE	High = Enable Low = Disable
--------	--------------------------------

**DMI Termination Voltage**

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH
--------	---

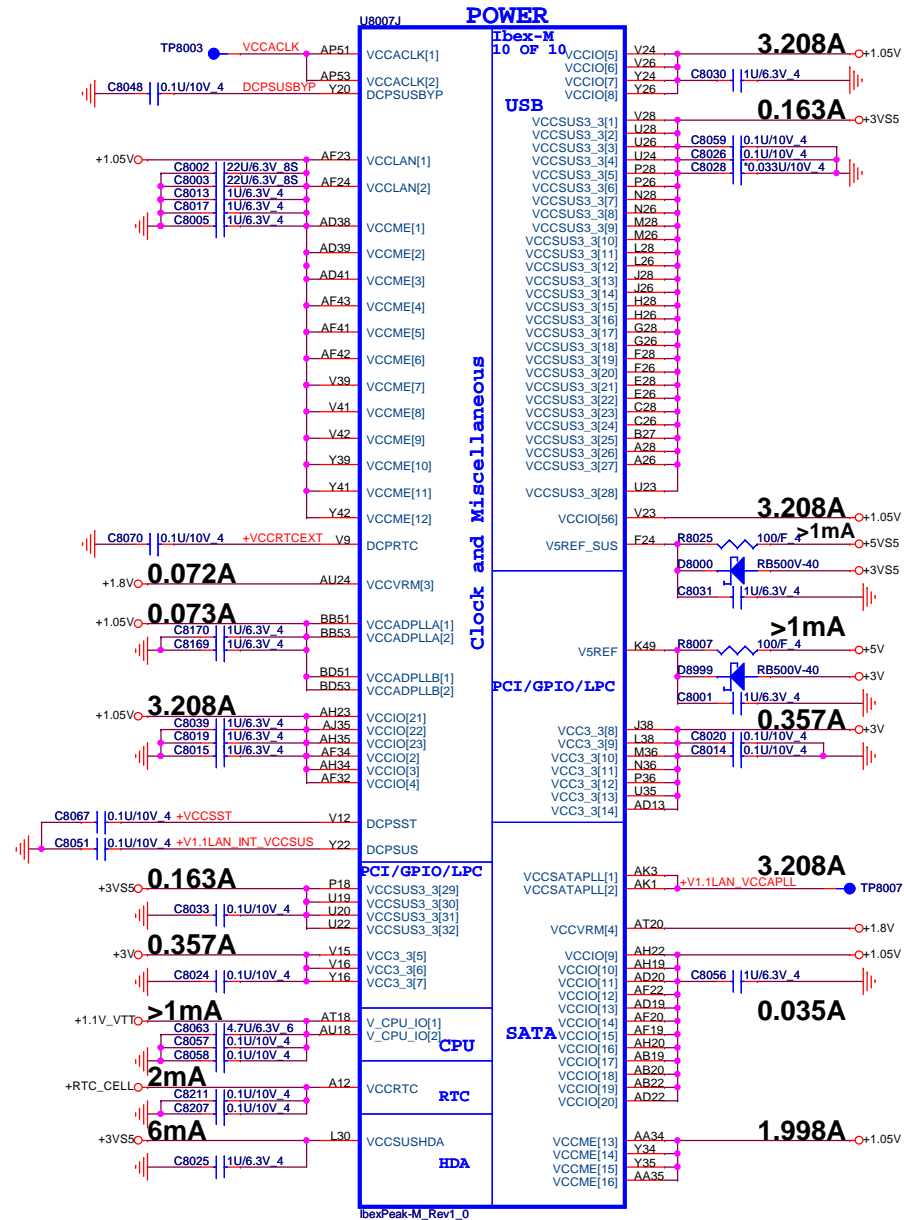
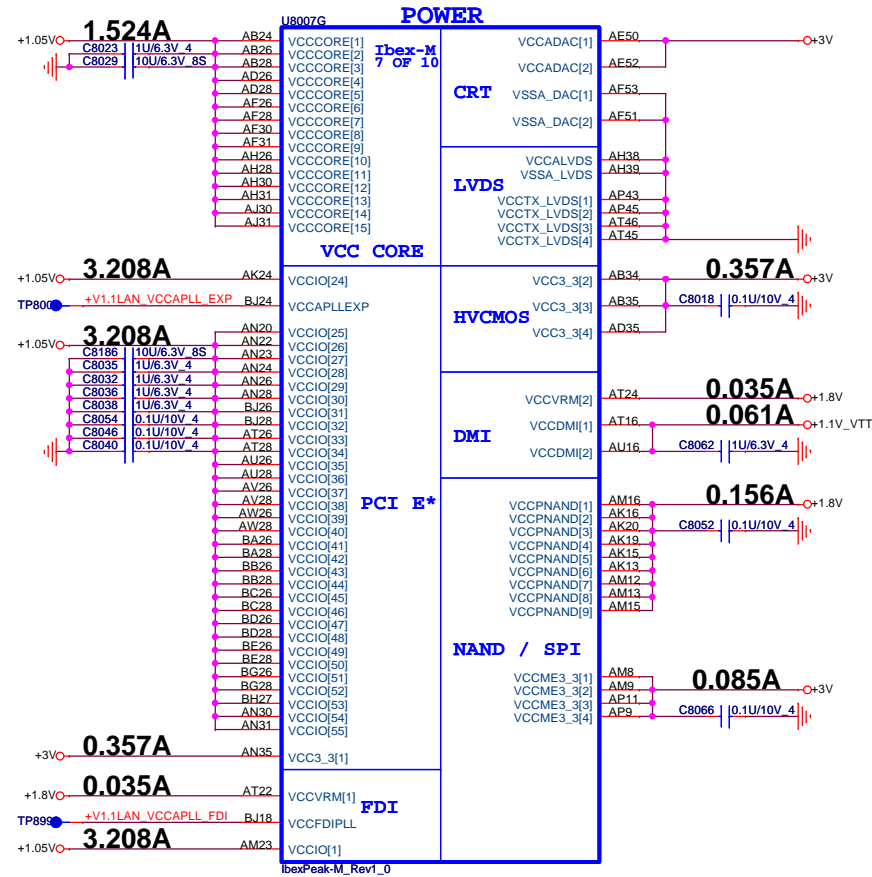
## No Reboot Strap



**PROJECT : SX6**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO & Strap)	2B

Date: Tuesday, December 15, 2009 | Sheet 11 of 43



3,8,9,10,34,39,41 +1.05V  
4,6,11,31,34,39,40 +1.1V\_VTT  
6,11,41,42 +1.8V  
3,4,8,9,10,11,14,15,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V  
4,9,10,11,29,31,32,33,34,38,41,42,43 +3V5S  
20,23,24,25,31,32,35,37,42 +5V  
23,35,36,37,38,40,42 +5V5S

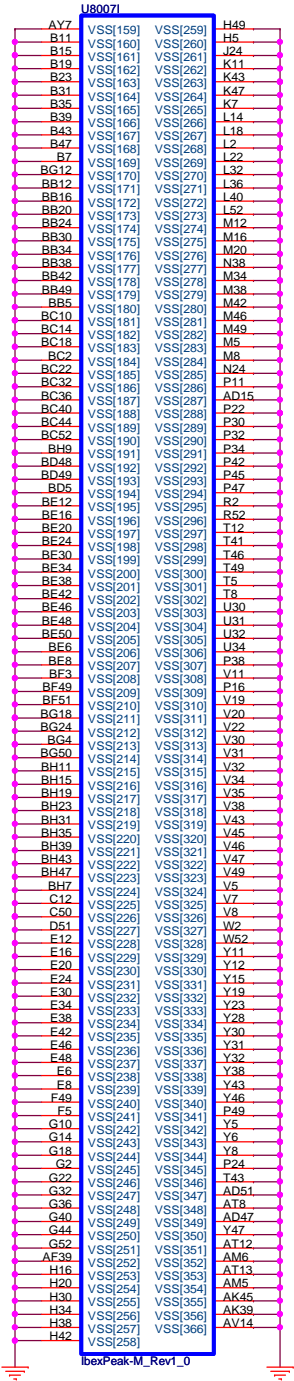


**PROJECT : SX6**  
**Quanta Computer Inc.**

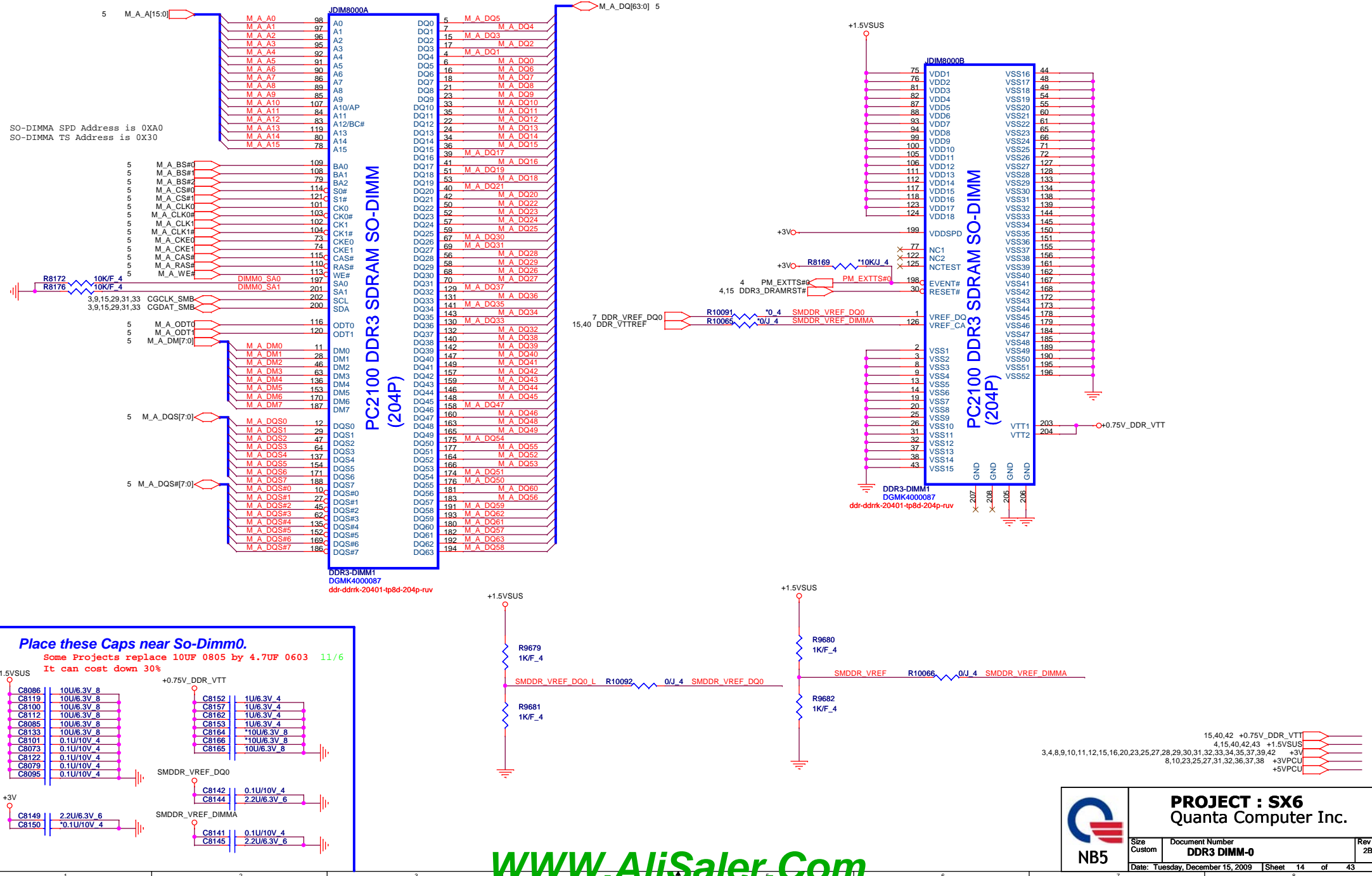
Size Custom	Document Number <b>PCH 5/6 (POWER)</b>	Rev 2B
Date: Tuesday, December 15, 2009   Sheet 12 of 43		

IBEX PEAK-M (GND)

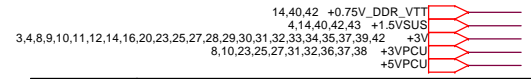
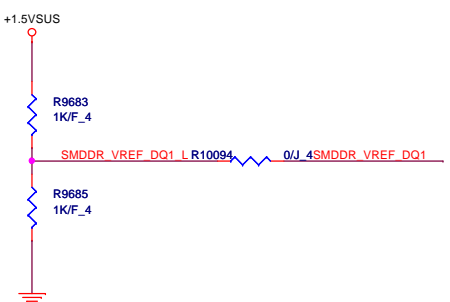
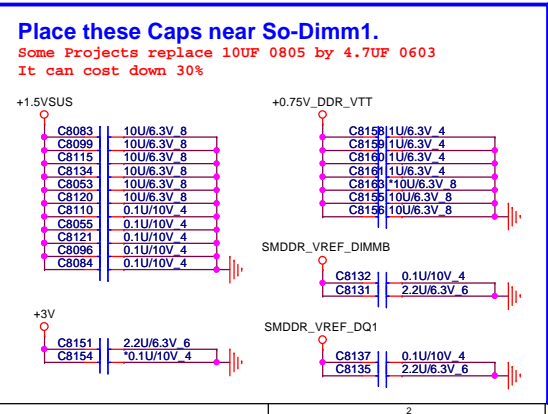
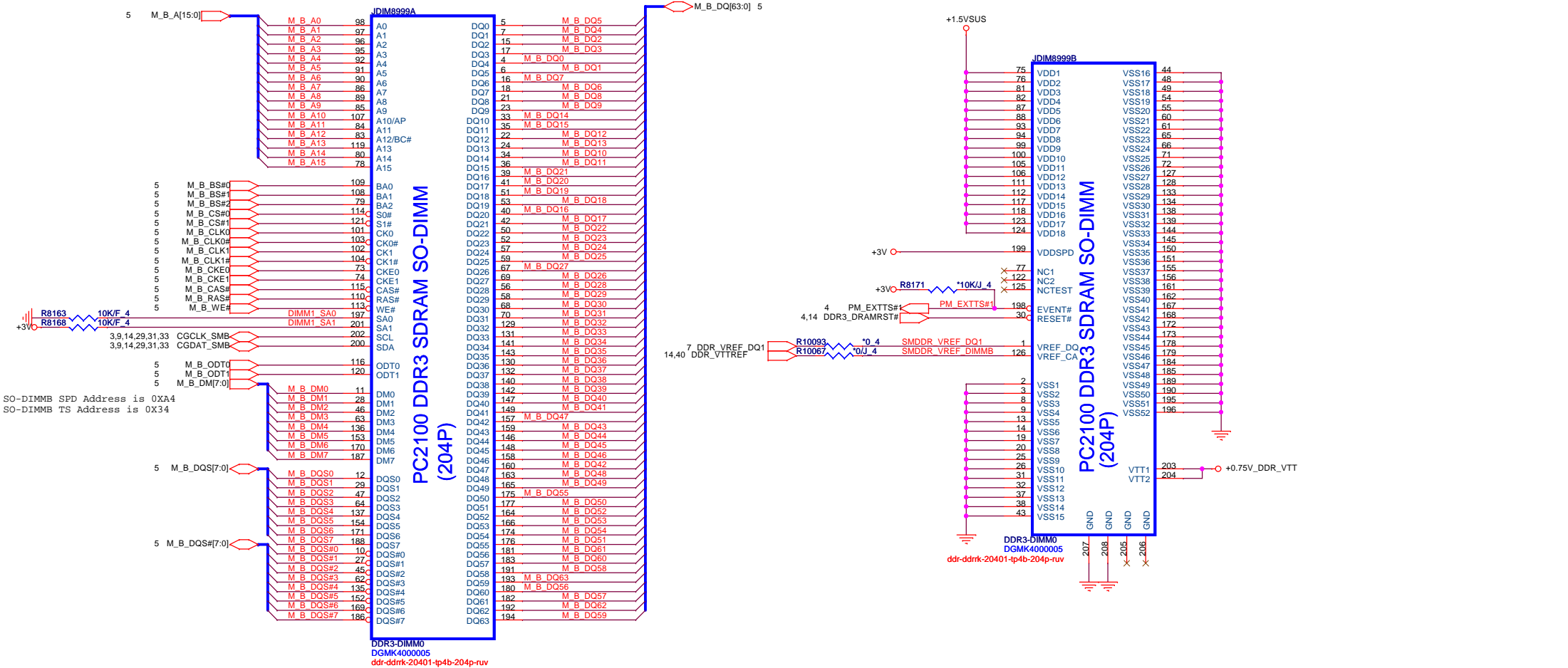
IBEX PEAK-M (GND)



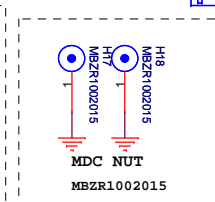
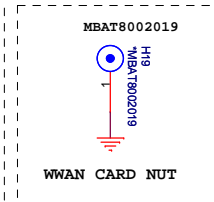
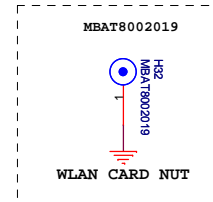
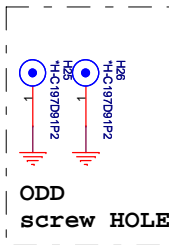
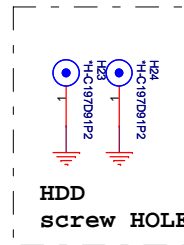
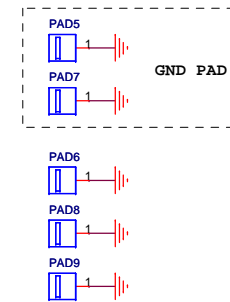
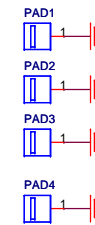
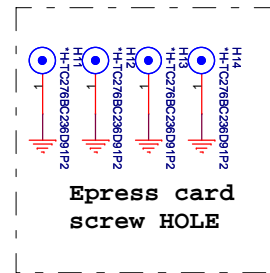
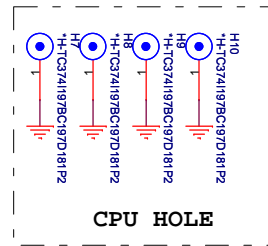
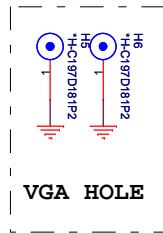
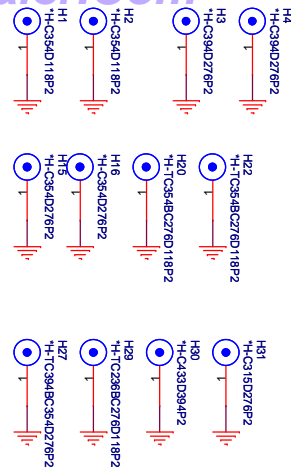




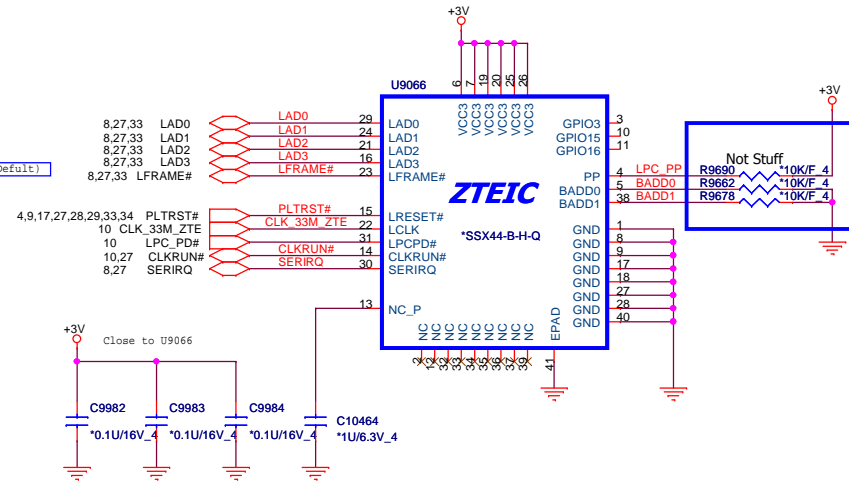
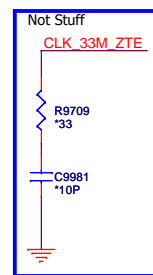


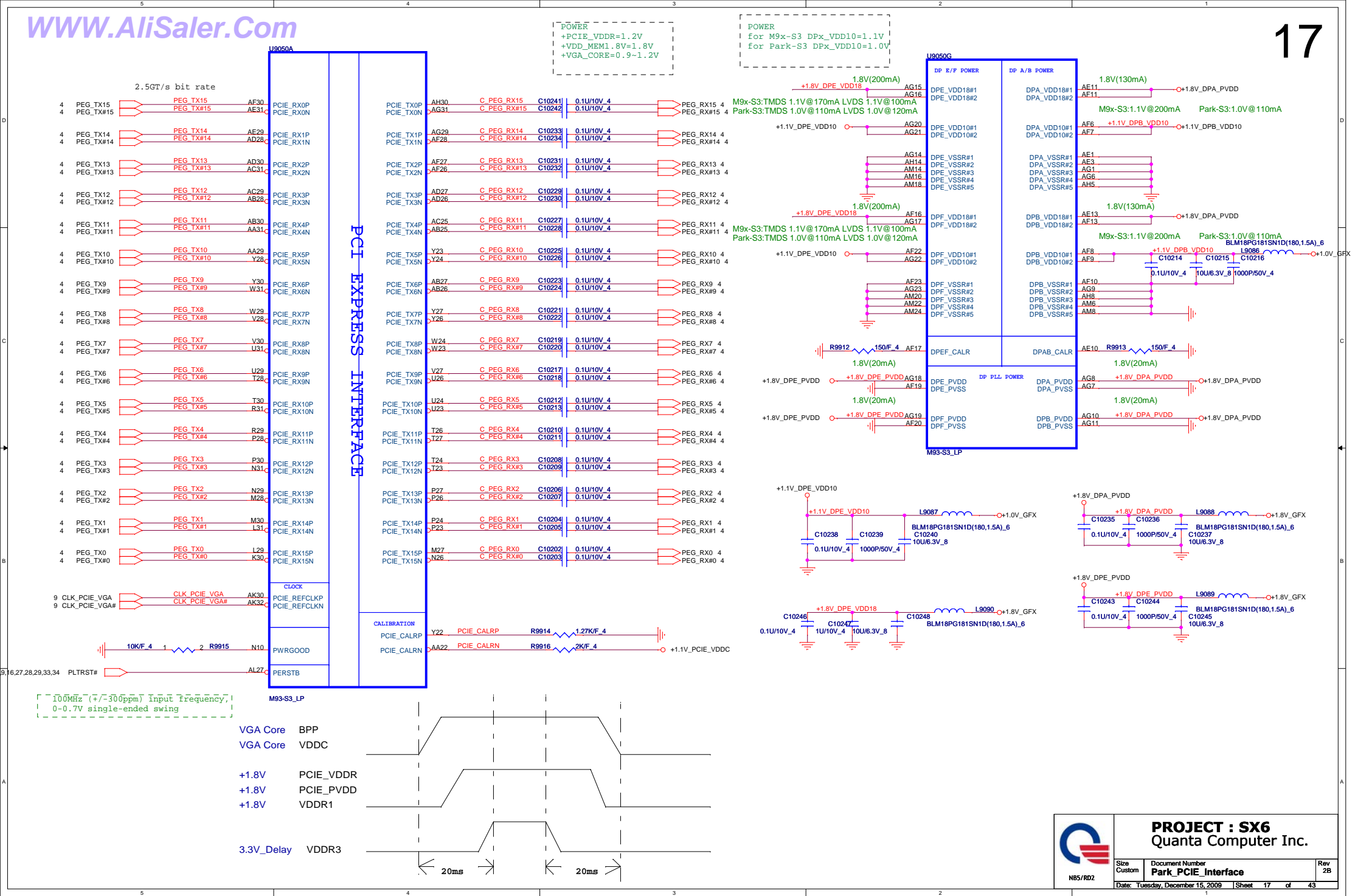


		<b>PROJECT : SX6</b> <b>Quanta Computer Inc.</b>	
		Size Custom Document Number <b>DDR3 DIMM-1</b>	Rev 2B
Date: Tuesday, December 15, 2009		Sheet 15 of 43	14,40,42 +0.75V_DDR_VTT 4,14,40,42,43 +1.5VSUS 3,4,8,9,10,11,12,14,16,20,23,25,27,28,29,30,31,32,33,34,35,37,39,42 +3V 8,10,23,25,27,31,32,36,37,38 +3VPCU +5VPCU

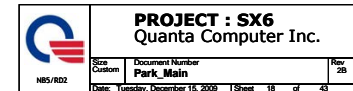


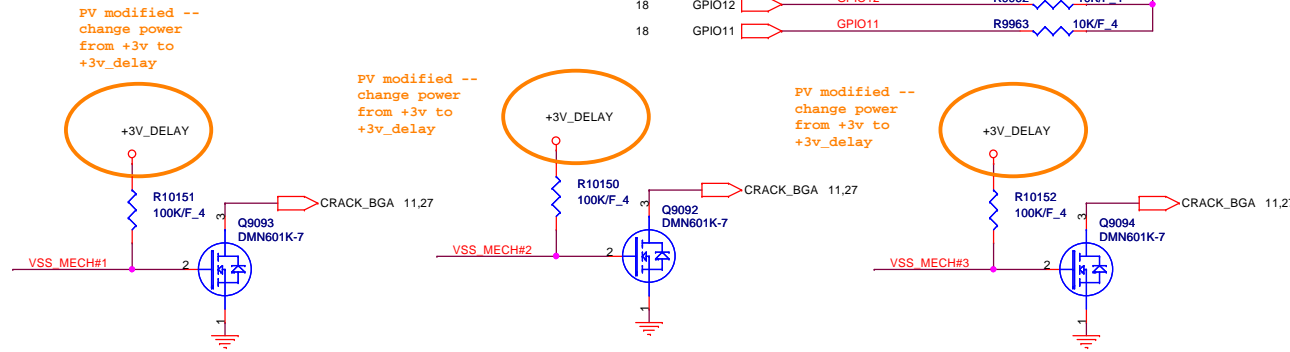
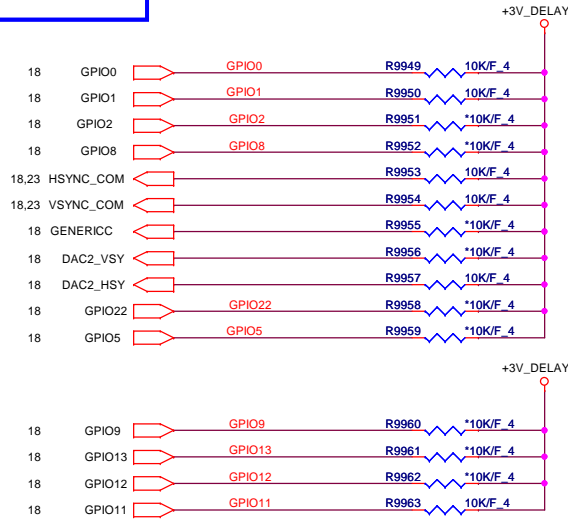
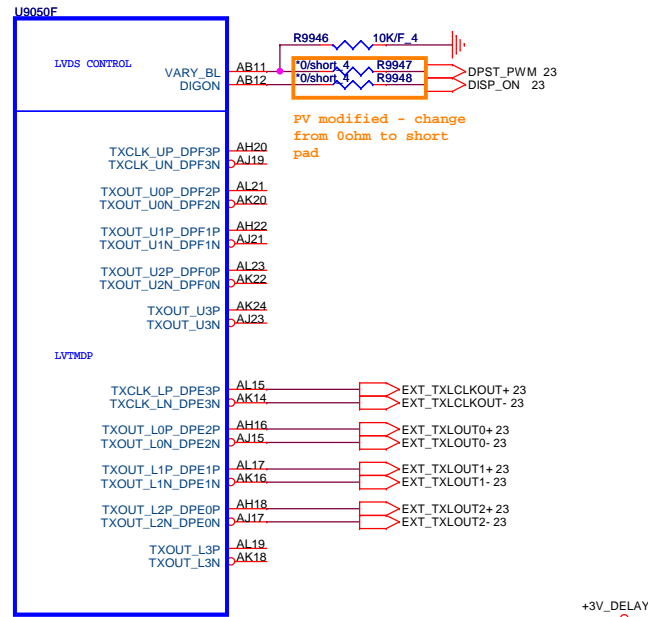
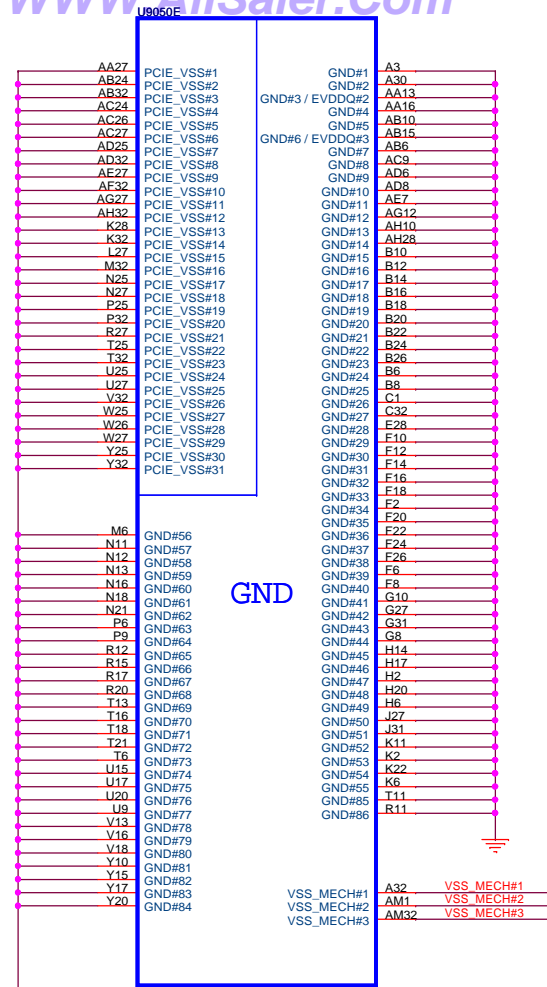
BADD1	BADD0
0	0
0	1
1	0
1	1





	BBEN	BBP
L	0	V-CORE
H	1	+1.8V





Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	PCI Express Full TX Output Swing 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD	GPIO8	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0]	VSYNC	AUD[1] AUD[0] 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1
AUD(1)	HSYNC		1
VIP_DEVICE_STRAP_ENA	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERICC		0

## Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

**PROJECT : SX6**  
Quanta Computer Inc.

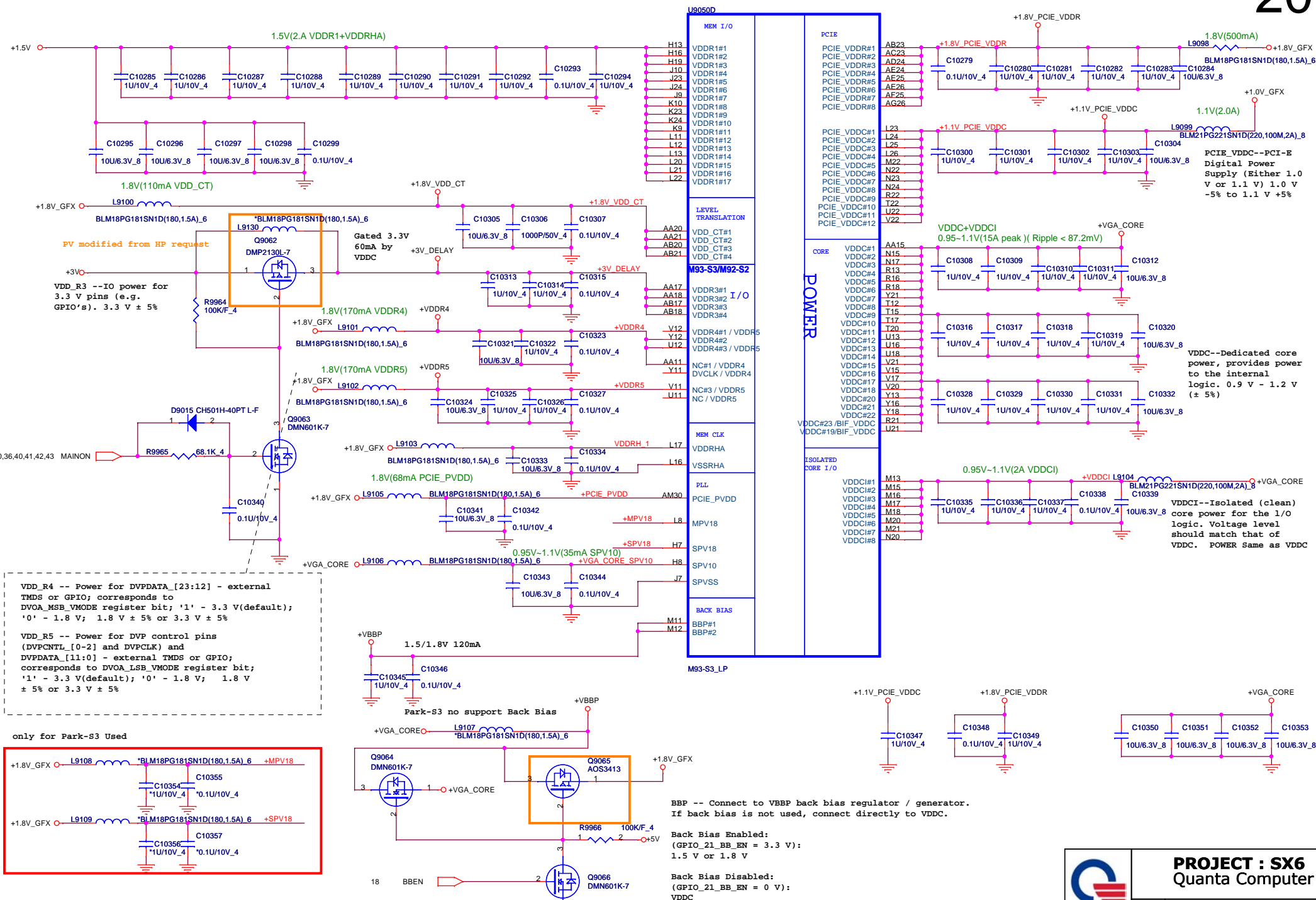
Size Custom

Document Number  
**Park\_GND / LVDS/ Straps**

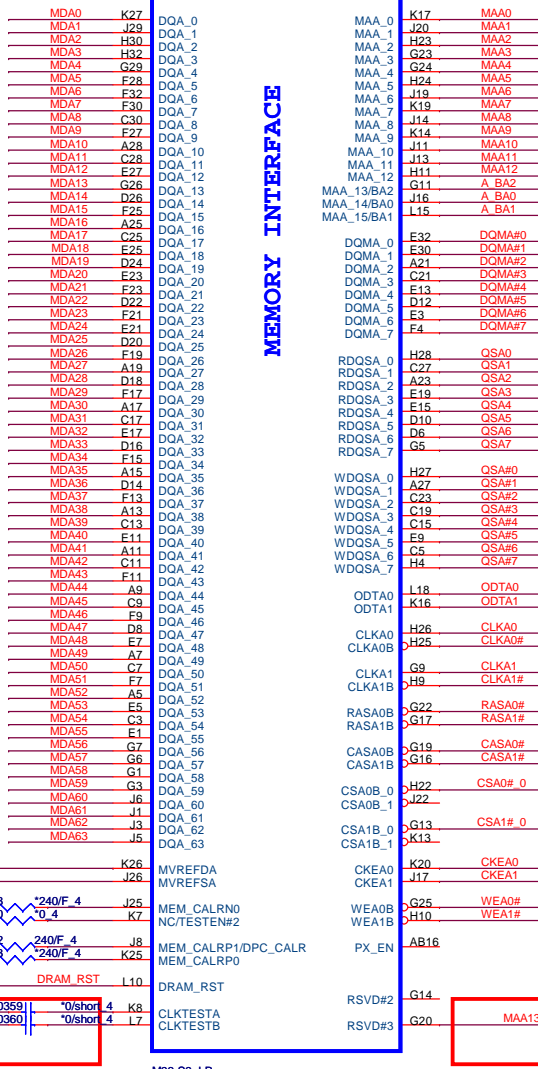
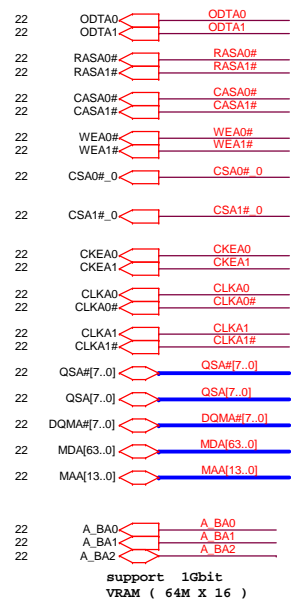
Date: Tuesday, December 15, 2009

Rev 2B

Sheet 19 of 43





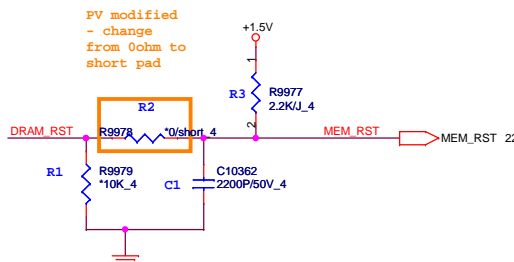


for Park-S3:Use only  
for M9x-S3: no support

for Park-S3:Use Cap 0.1uF, Res 51.1R  
for M9x-S3:Use Cap 0R, Res 4.7K

	M9x-S2/S3	Park-S3
MEM_CALRN0 (J25)	NC	240R
MEM_CALRP0 (K25)	NC	0R
MEM_CALRP1 (J8)	240R	150R
TESTEN2#2 (K7)	NC	0R
R1	NC	10K
R2	0R	680R
R3	2.2K	NC
C1	2.2nF	68pF

240R:CS12402FB03  
150R:CS11502FB21  
  
0R:CS00002JB38  
680R:CS16802JB27  
  
2.2nF:CH22206KB16  
68pF:CH06806JB01

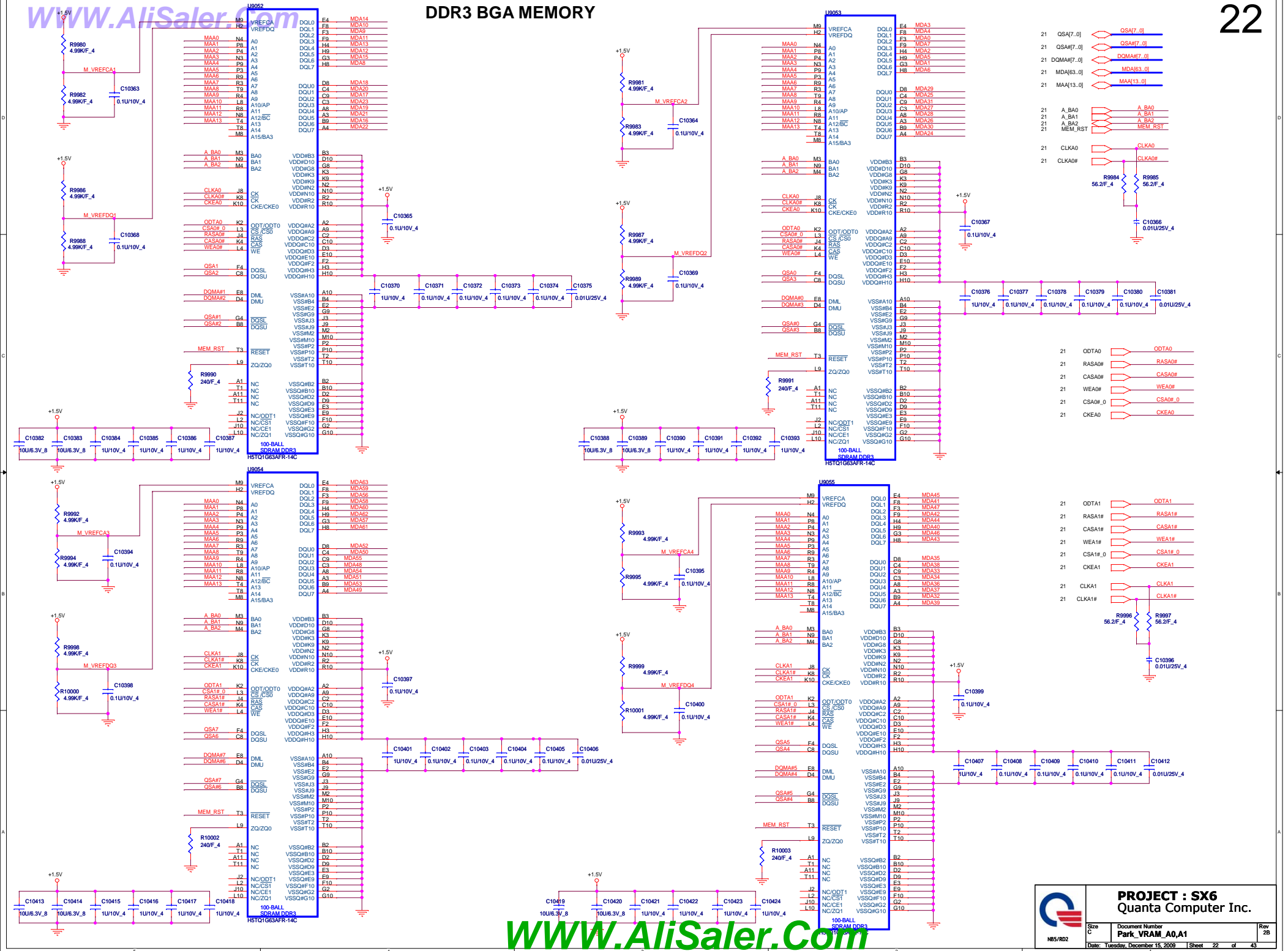


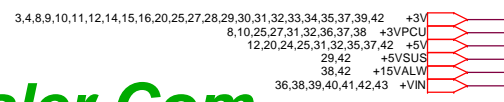
**PROJECT : SX6**  
Quanta Computer Inc.

Size Custom	Document Number <b>Park_MEM_Interface</b>	Rev 2B
Date: Tuesday, December 15, 2009 Sheet 21 of 43		

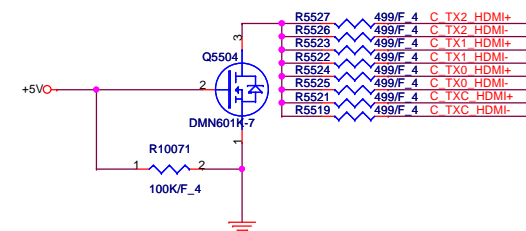
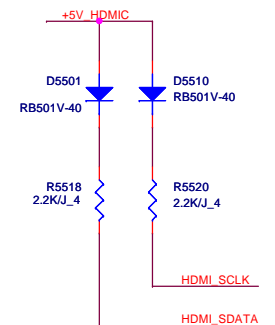
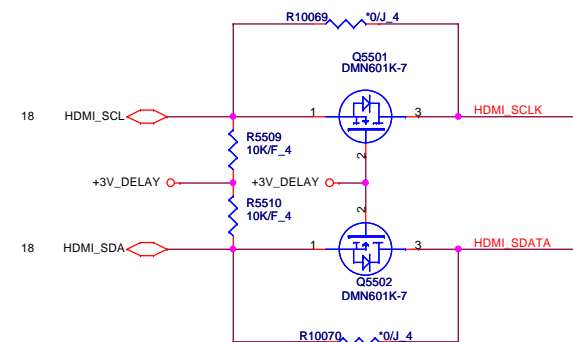
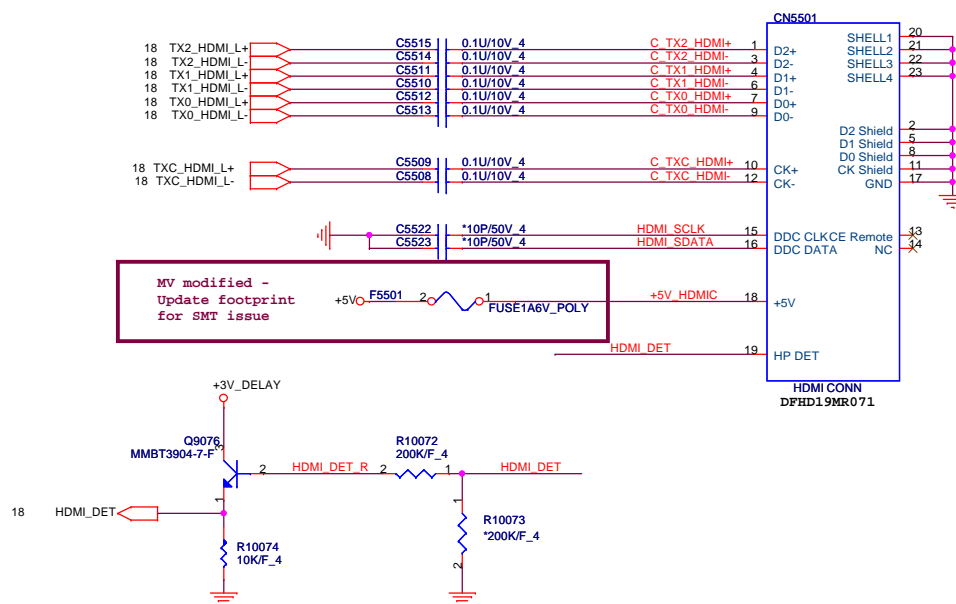
# DDR3 BGA MEMORY

22

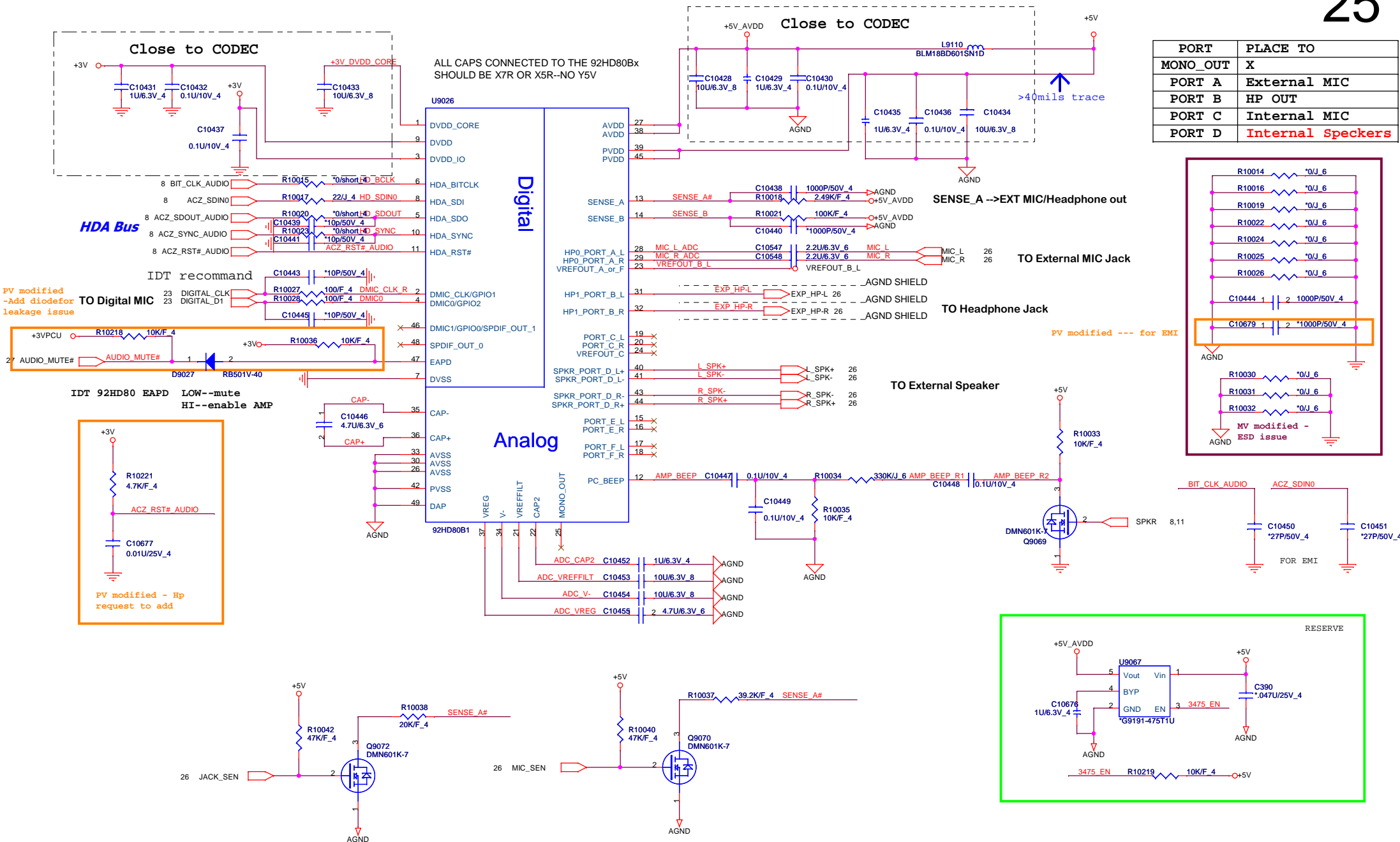




**WWW.AliSaler.Com**



PORT	PLACE TO
MONO_OUT	X
PORT A	External MIC
PORT B	HP OUT
PORT C	Internal MIC
PORT D	Internal Speckers

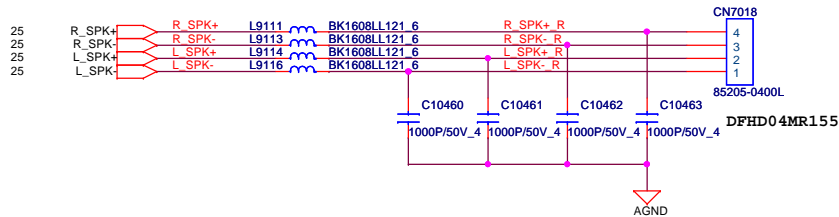


**PROJECT : SX6**  
Quanta Computer Inc.

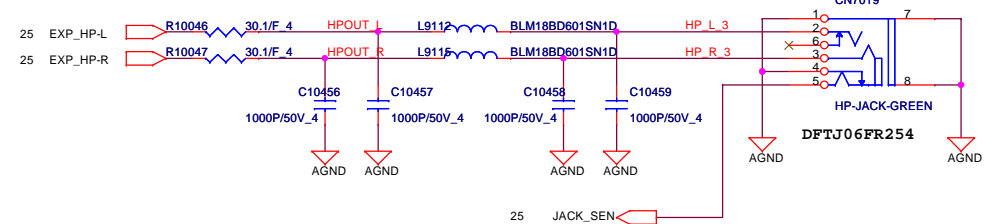
Size Custom	Document Number <b>IDT92HD80</b>	Rev 2B
Date: Thursday, December 17, 2009   Sheet 25 of 43		

Note: JACK\_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

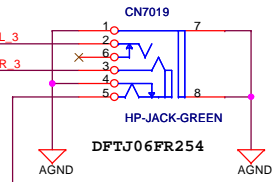
### INT. SPEAKER



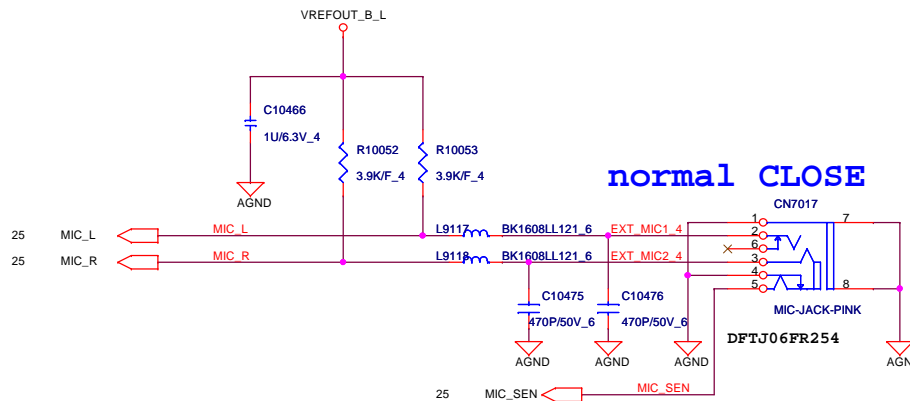
### Headphone Jack



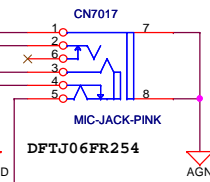
### normal CLOSE




### EXT Mic Jack



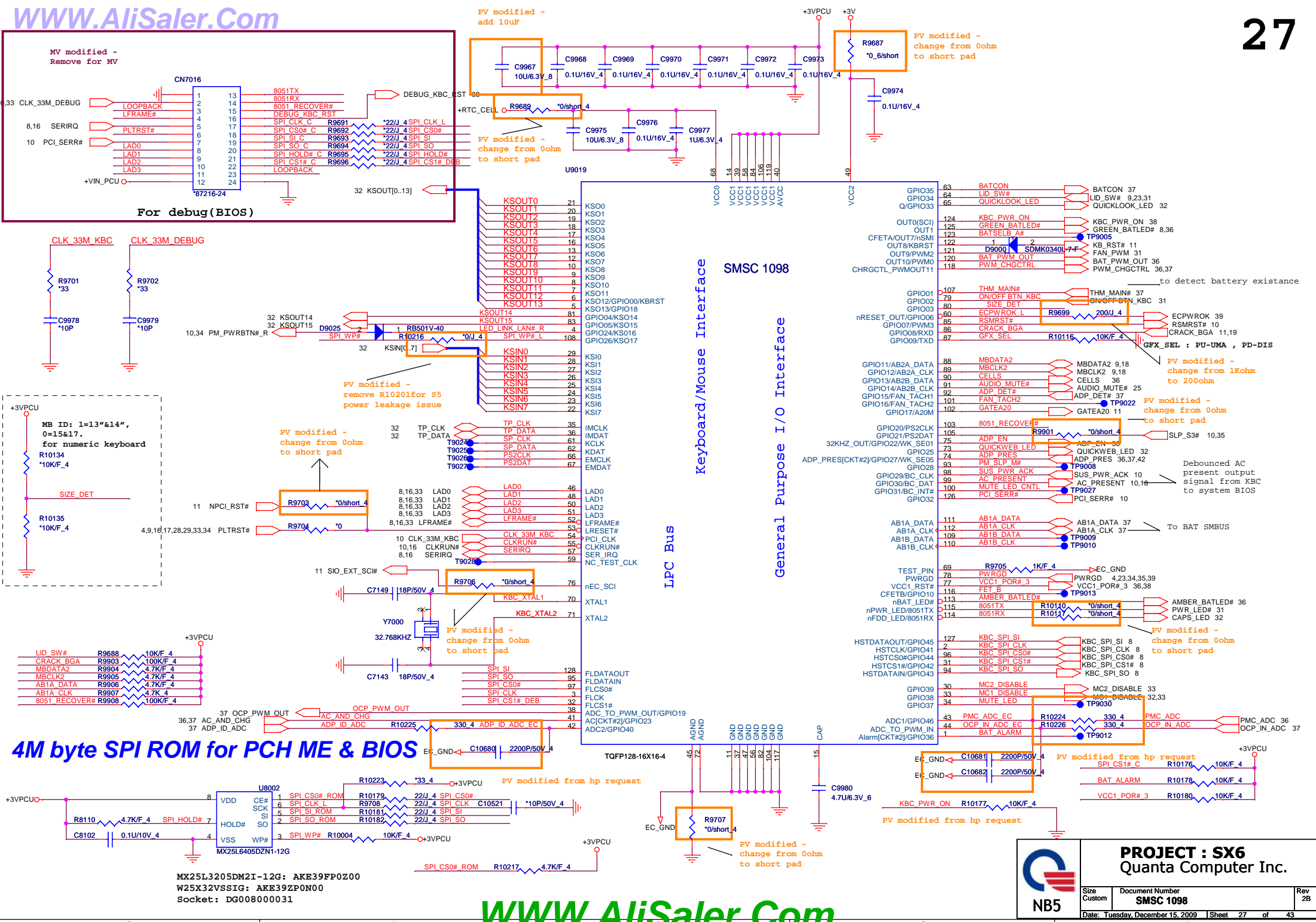
### normal CLOSE

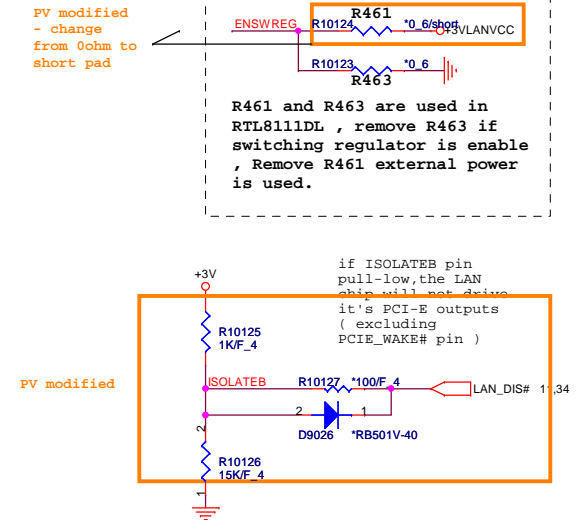
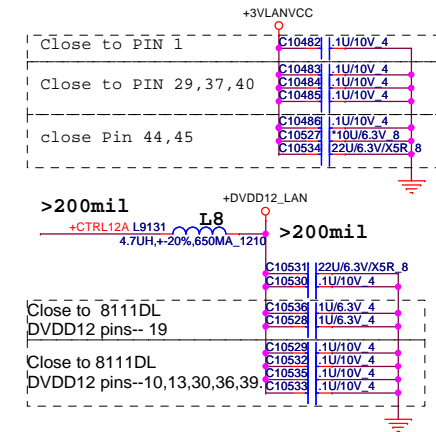


Note: MIC\_SEN# is electrically floating when no jack is inserted and shorted to ground when jack is present.

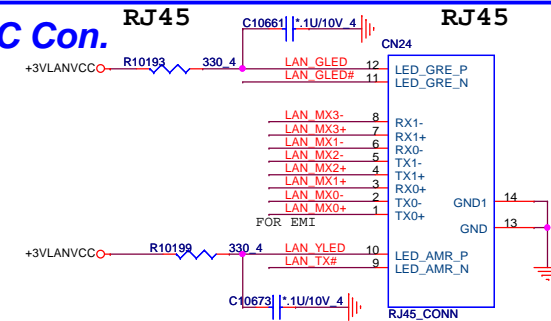
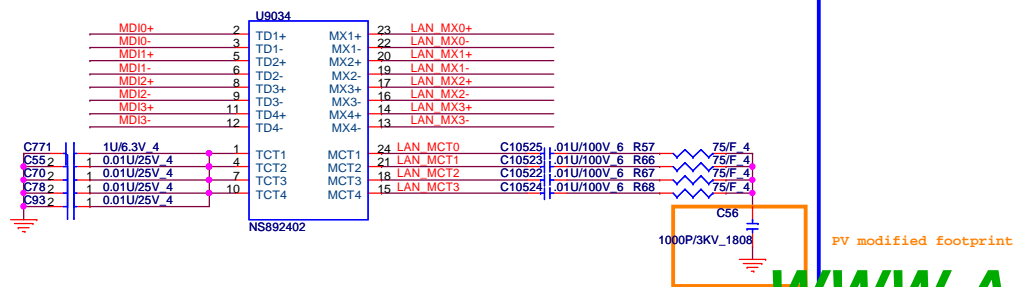
	<b>PROJECT : SX6</b> Quanta Computer Inc.	
	Size Custom Document Number <b>HP/MIC/SPK</b> Date: Tuesday, December 15, 2009	Rev 2B Sheet 26 of 43







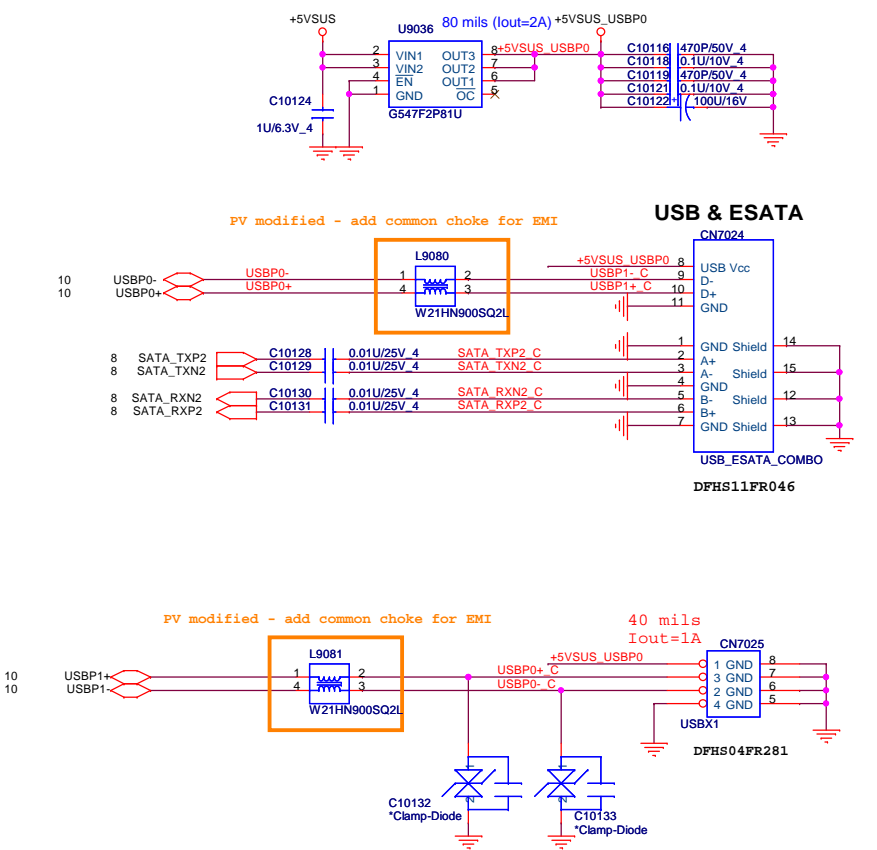
## RJ45



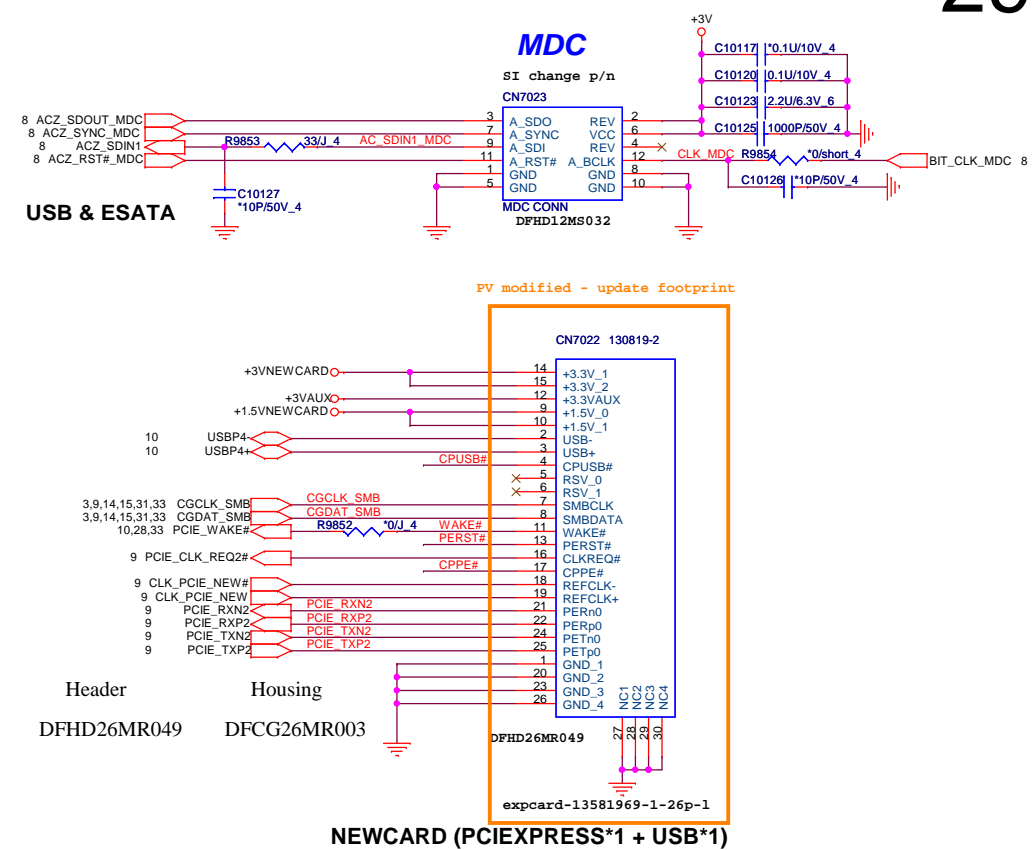
**PROJECT : SX6**  
Quanta Computer Inc.

Size Custom	Document Number <b>RTL8151DH-GR</b>	Rev 2B
Date: Friday, December 18, 2009		Sheet 28 of 43

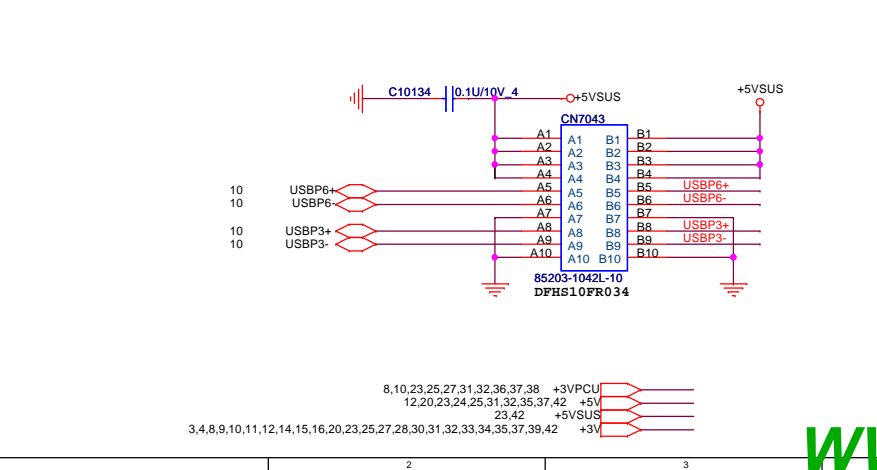
LEFT SIDE USBX1 and E-SATA/USB COMBO



Modem CONN



RIGHT SIDE USBX2



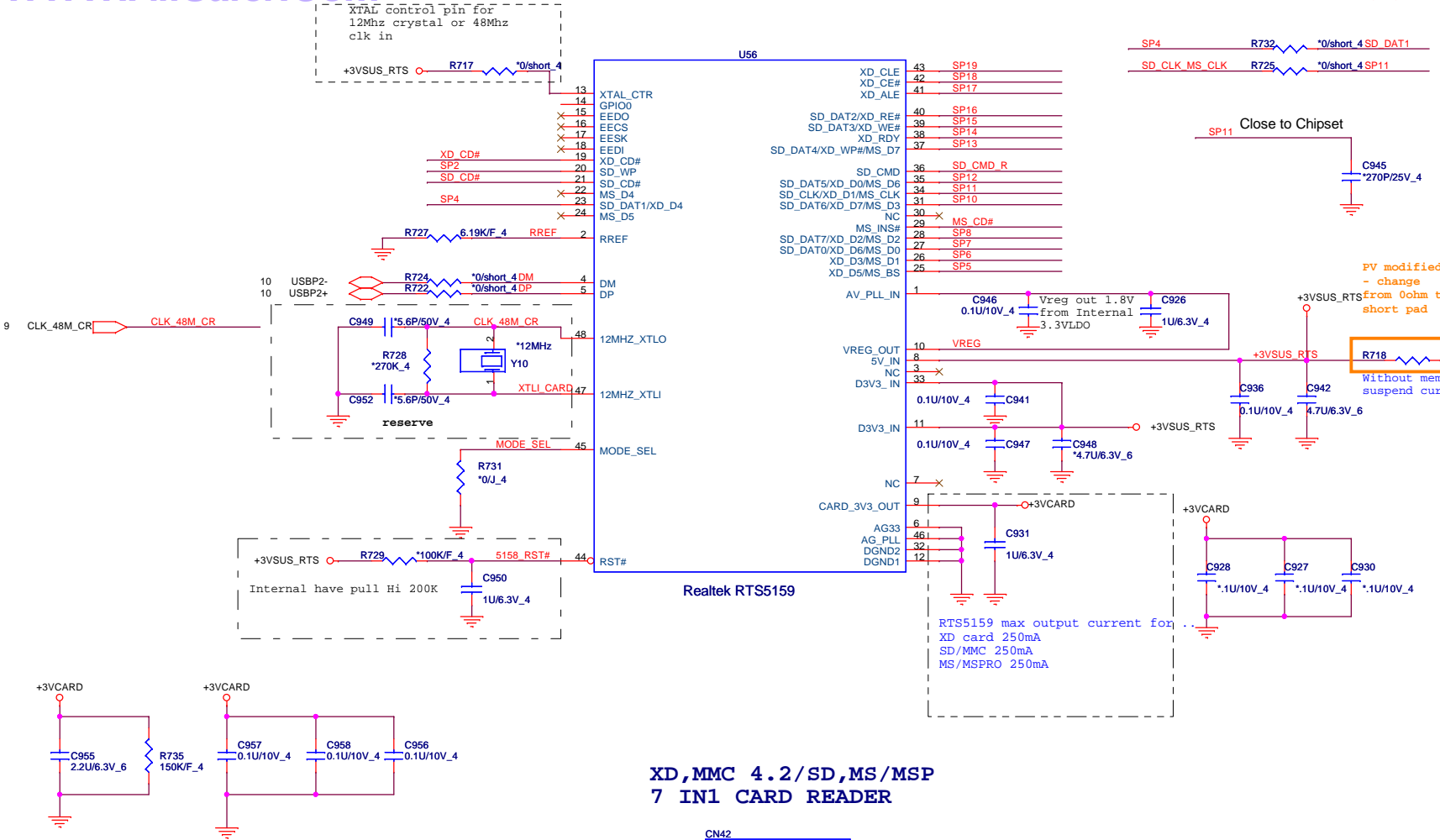
**PROJECT : SX6**  
Quanta Computer Inc.

Size Custom	Document Number	Rev
	<b>EXTERNAL USB X2</b>	2B
Date: Wednesday, December 16, 2009		Sheet 29 of 43

NB5

Note:

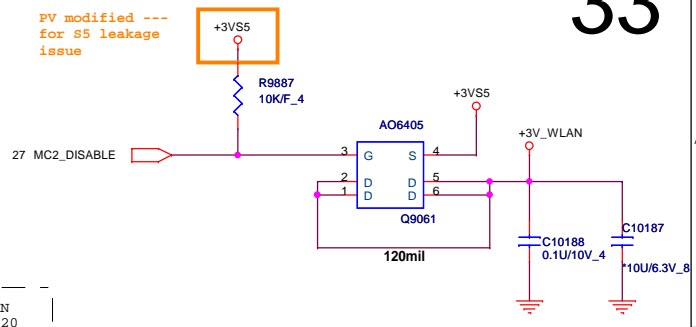
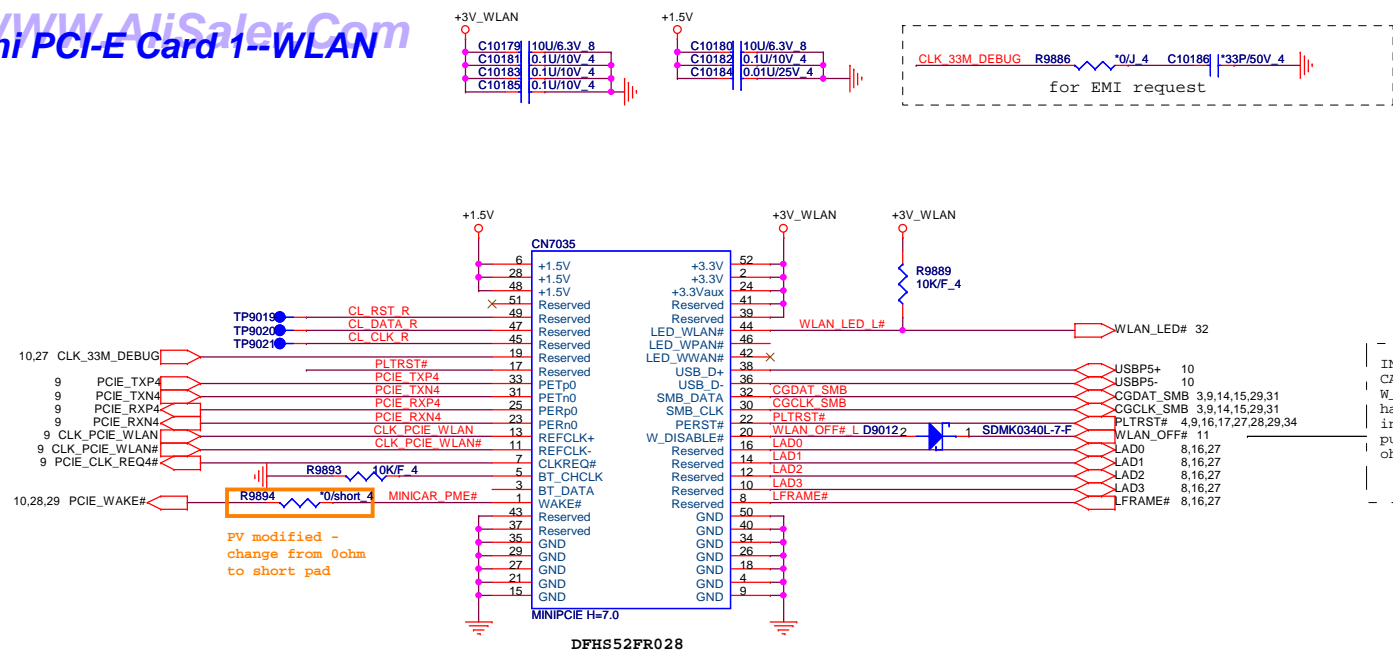
SD/MMC 4.2	MS	XD
SP0		XD CD#
SP1	SD WP	
SP2	SD CD#	
SP3	SD DAT1	XD D4
SP4		XD D5
SP5	MS BS	XD D6
SP6	MS D1	XD D7
SP7	MS D0	XD D8
SP8	SD DAT7/MMC DAT7	XD D9
SP9	MS INS#	
SP10	SD DAT6/MMC DAT6	XD D10
SP11	SD CLK	XD D11
SP12	SD DAT5/MMC DAT5	XD D12
SP13	SD DAT4/MMC DAT4	XD WP#
SP14		XD R/B#
SP15	SD DAT3	XD WE#
SP16	SD DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE



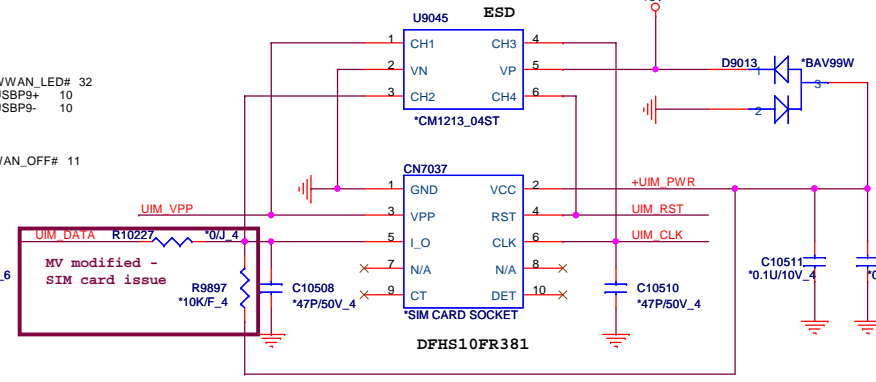
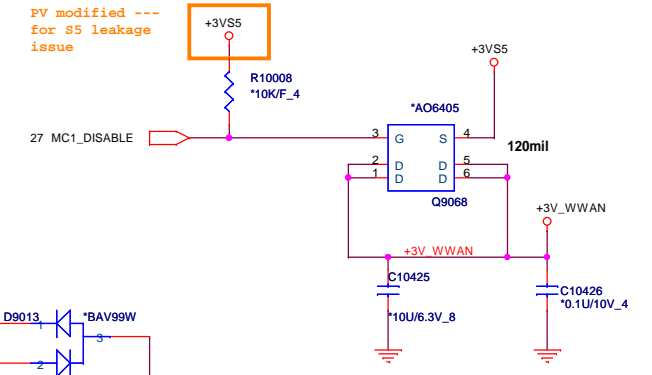
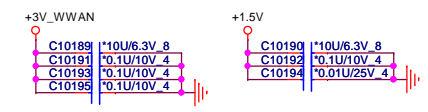
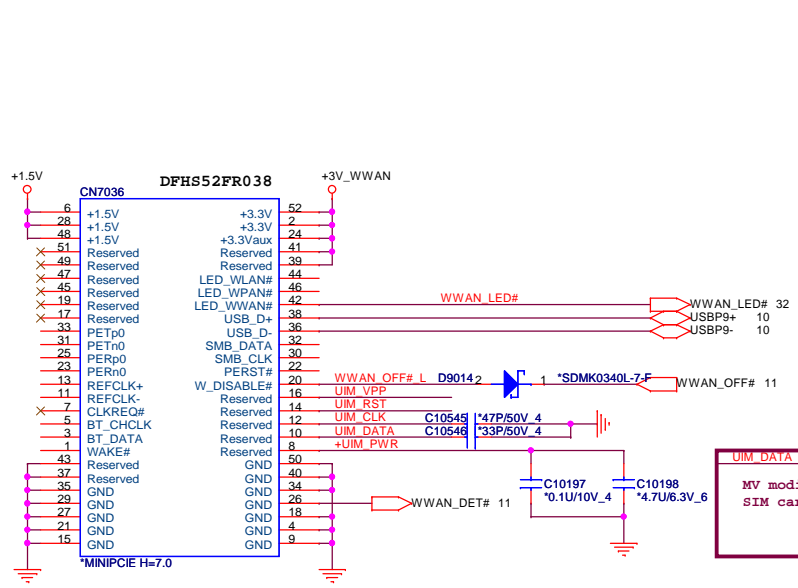






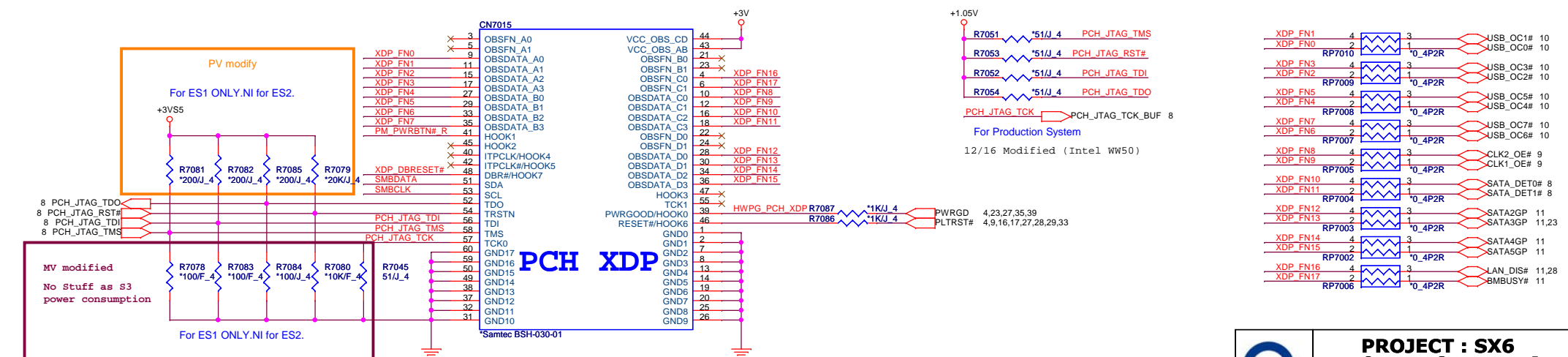
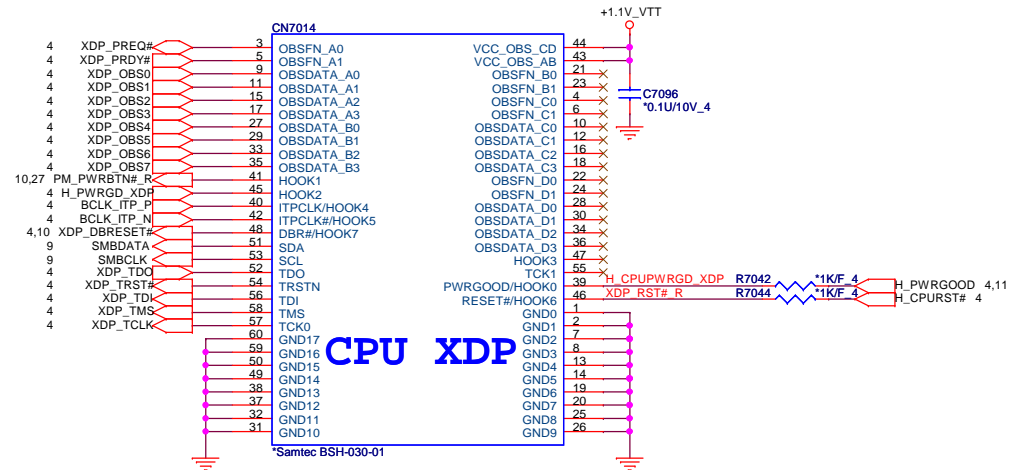


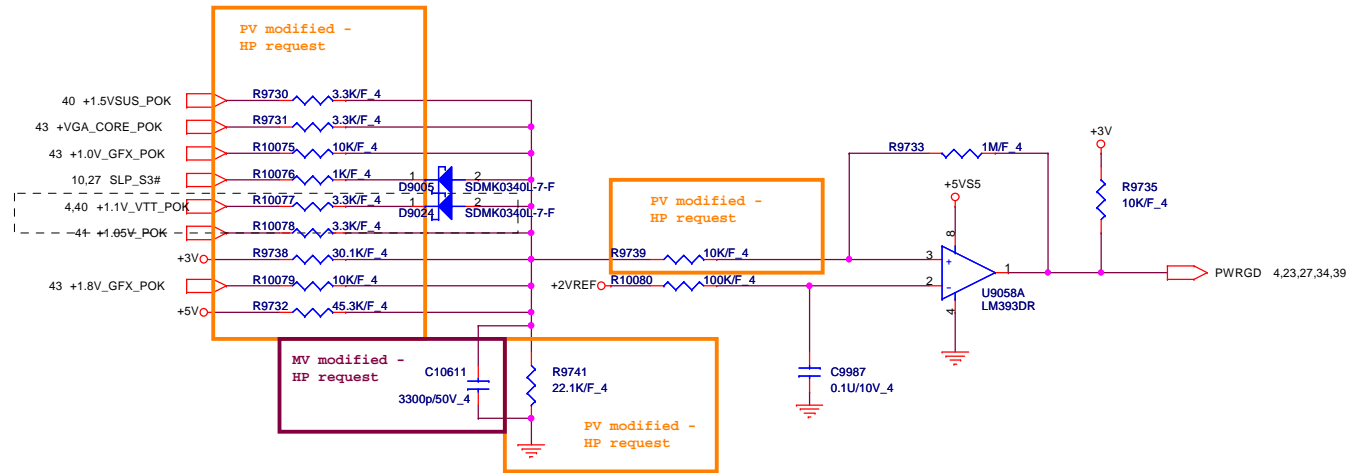
Mini PCI-E Card 2 --WWAN

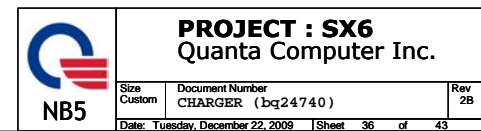


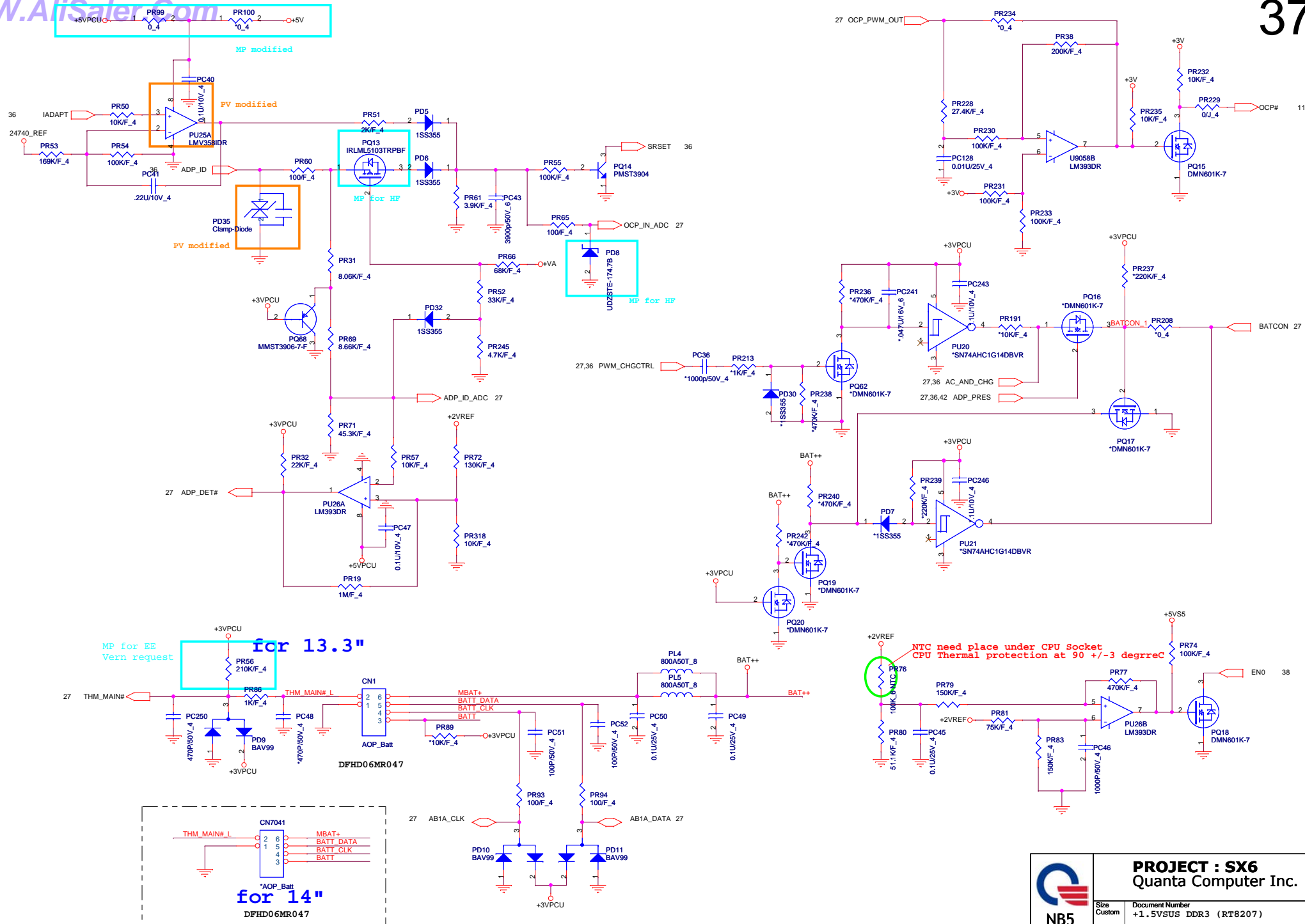
**PROJECT : SX6**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2	2B
Date: Tuesday, December 15, 2009   Sheet 33 of 43		





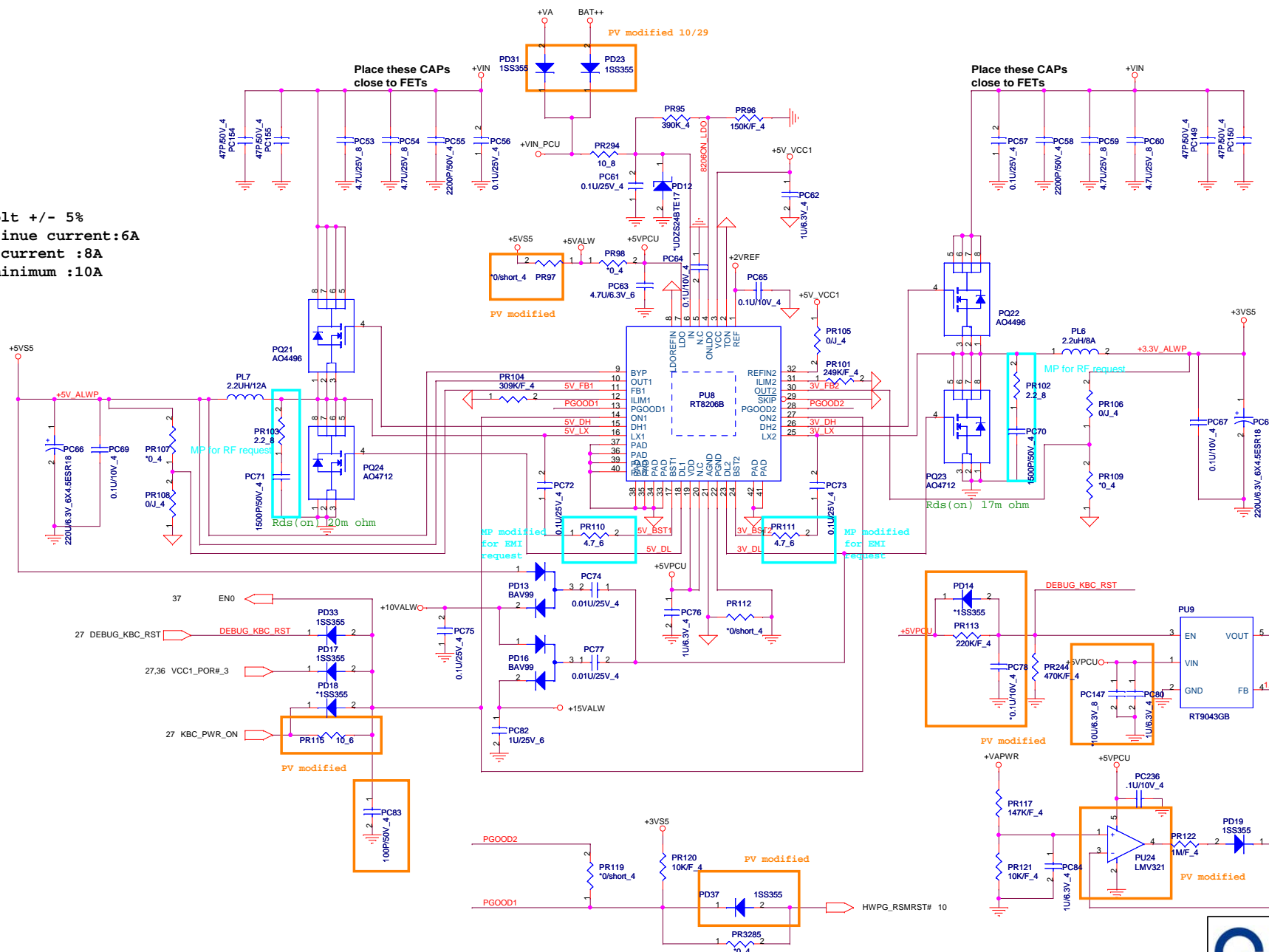




+5 Volt +/- 5%  
Countinue current:6A  
Peak current :8A  
OCP minimum :10A

+3.3 Volt +/- 5%  
Countinue current:5A  
Peak current:6A  
OCP minimum 7.5A

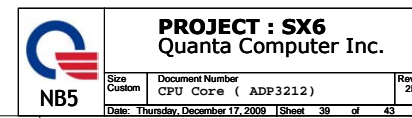
+3.3 Volt +/- 5%  
Countinue current: 100mA

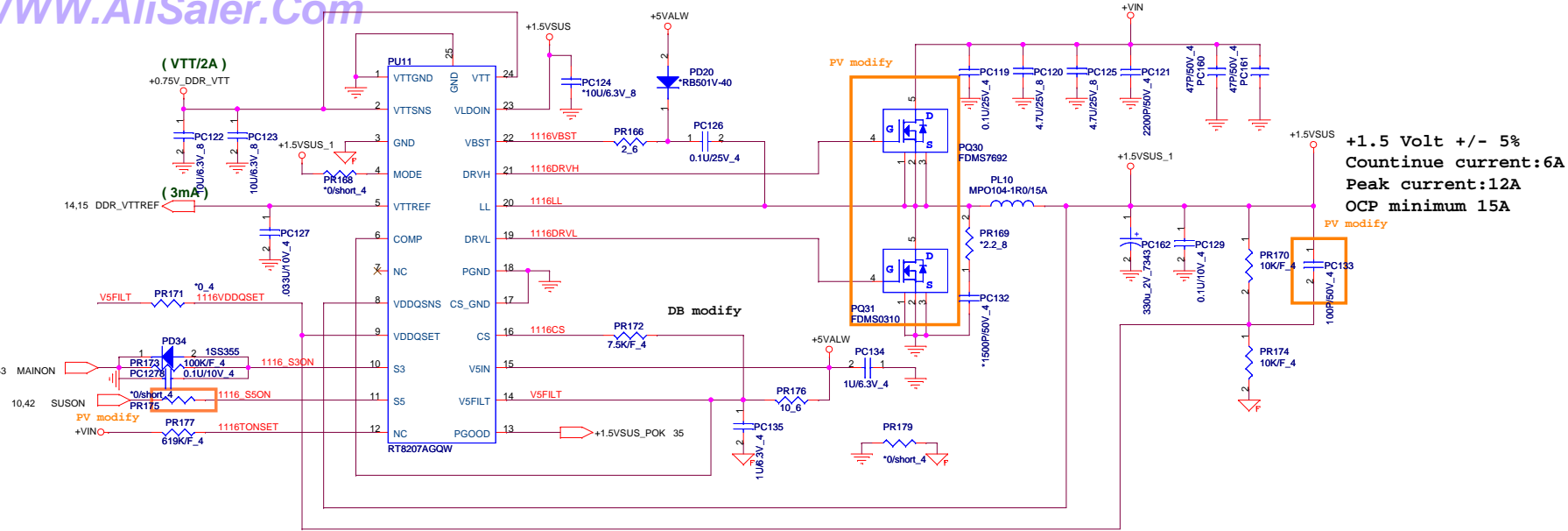


**PROJECT : SX6**  
Quanta Computer Inc.

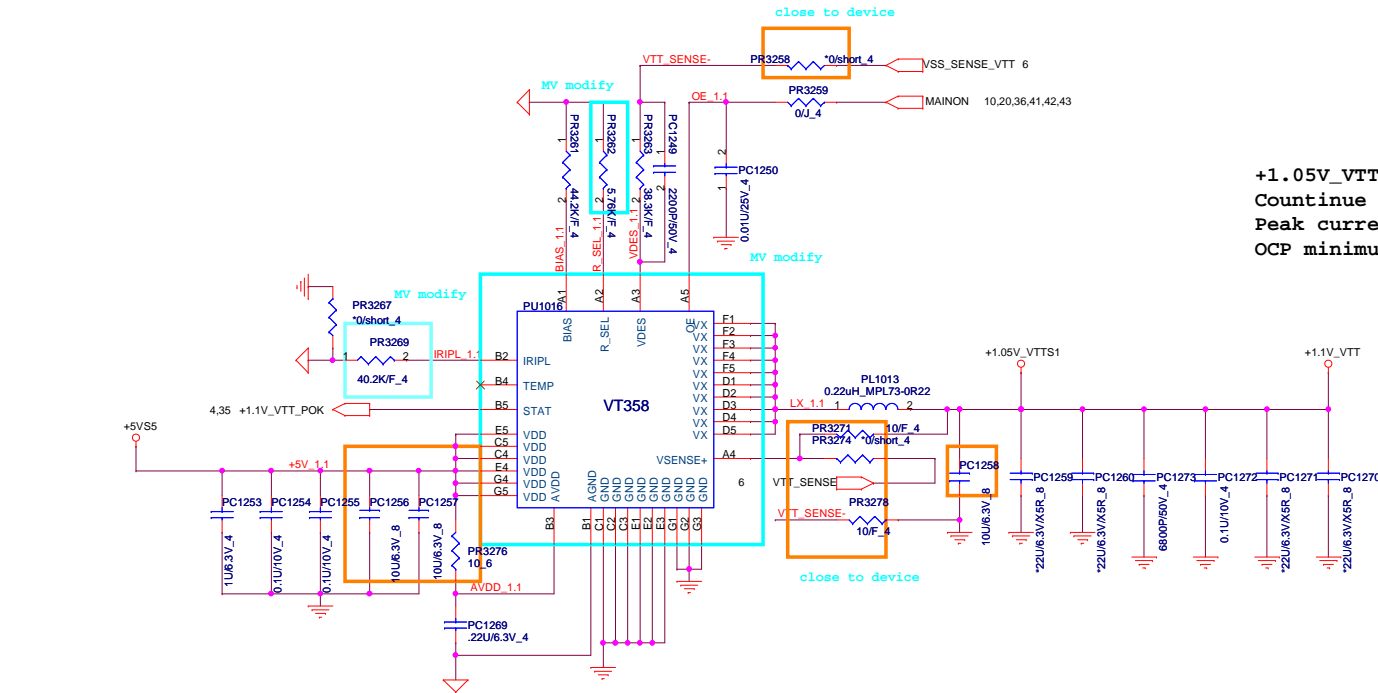
Size Custom	Document Number +5V/+3V (RT8206B)	Rev 2B
Date: Thursday, December 17, 2009   Sheet 36 of 43		






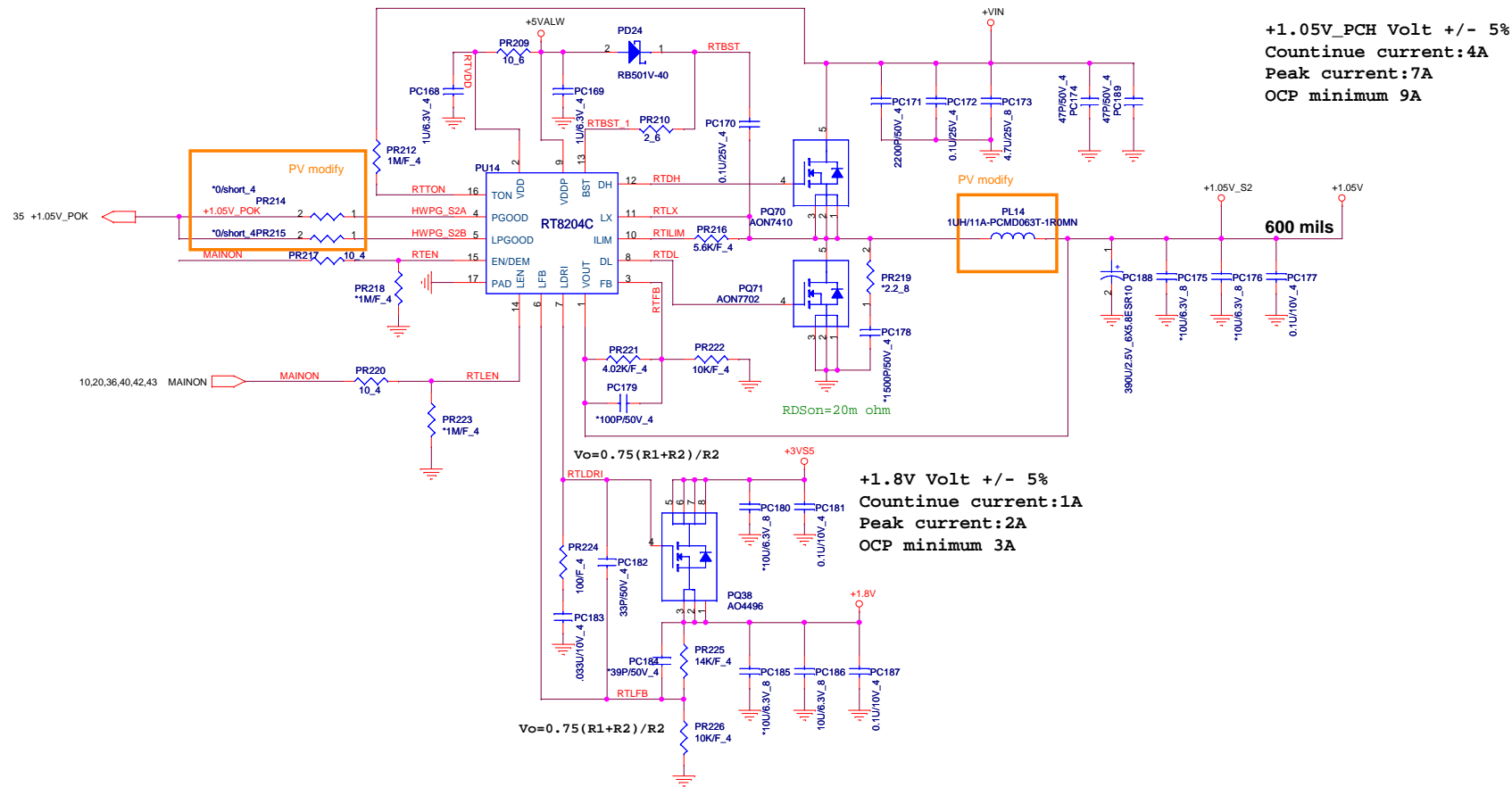


**+1.5 Volt +/- 5%**  
**Countinue current:6A**  
**Peak current:12A**  
**OCp minimum 15A**

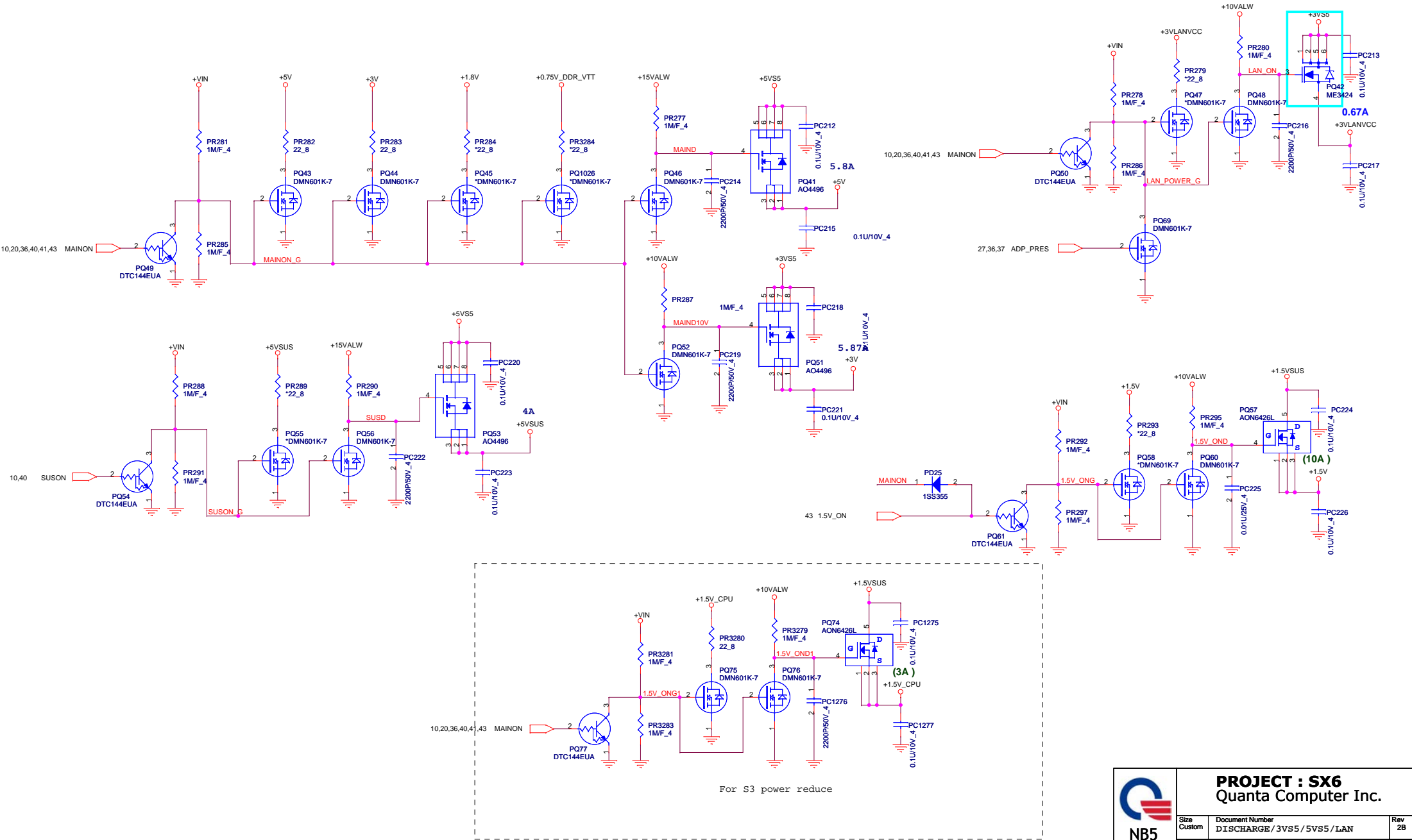



**+1.05V\_VTT +/- 5%**  
**Countinue current:12A**  
**Peak current:15A**  
**OCp minimum 18A**

	<b>PROJECT : SX6</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3 (RT8207)	Rev 2B
	Date: Thursday, December 17, 2009	Sheet 40	of 43



MP改无刷跟ESD





**PROJECT : SX6**  
Quanta Computer Inc.

Size Custom	Document Number DISCHARGE / 3VS5 / 5VS5 / LAN	Rev 2B
Date: Thursday, December 17, 2009   Sheet 42 of 43		

# VGA Core & VCC1.1

	PWRCNTL1	PWRCNTL0	V-CORE
	1	1	0.9V
	1	0	0.95V
	0	1	1.05V
	0	0	1.1V

